General Description

The DA16200MOD is a fully integrated Wi-Fi® module with ultra-low power consumption, best RF performance and easy development environment. Such low power operation can extend the battery life as longer as a year or more depending on the application.

This module series included DA16200-00000A32, 40 MHz crystal oscillator, 32.768 KHz RTC clock, RF Lumped RF filter, 4 M-byte flash memory and chip antenna or u.FL connector. The DA16200MOD has chip antenna type (DA16200MOD-AAC4WA32) and u.FL connector type (DA16200MOD-AAE4WA32) for external antenna.

The Module is built from the ground up for the Internet of Things (IoT) and is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video door bells, wearables and other IoT devices.

The modules certified Wi-Fi alliance for IEEE802.11b/g/n, Wi-Fi Direct, WPS functionalities and it has been approved by many countries including the United States (FCC), Canada (IC) and China (SRRC). Using the Wi-Fi Alliance transfer policy, the Wi-Fi Certifications can be transferred without being tested again.
For more information on DA16200MOD, please refer to DA16200-00000A32 datasheet.

Key Features

- Module variants
  - DA16200MOD-AAC4WA32 (chip Antenna)
  - DA16200MOD-AAE4WA32 (u.FL cont.)
- Highly integrated ultra-low power Wi-Fi® system module
  - Sleep current: 3.5 uA, VBAT=3.3 V
- Best RF Performance
  - Tx Power: +19 dBm, 1 Mbps DSSS
  - Rx Sensitivity: -98.5 dBm, 1 Mbps DSSS
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
  - IEEE 802.11b/g/n, 1x1, 20 MHz channel bandwidth, 2.4 GHz
  - IEEE 802.11s Wi-Fi mesh
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station, SoftAP, and Wi-Fi Direct® Modes (GO, GC, GO fixed)
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Connection manager for autonomous and fast Wi-Fi connections
  - Bluetooth coexistence
  - Antenna switching diversity
- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: single-ended four channels
  - Provides dynamic auto switching function
- Supports various interfaces
  - eMMC/SD expanded memory
  - SDIO Host/Slave function
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- Wi-Fi Alliance certifications:
  - Wi-Fi CERTIFIED™ b, g, n
  - WPA™ - Enterprise, Personal
  - WPA2™ - Enterprise, Personal
  - WPA3™ - Enterprise, Personal
- RF Regulatory certifications
  - FCC, IC, CE, KC, TELEC, SRRC
- CPU core subsystem
  - Arm® Cortex®-M4F core w/ clock frequency of 30~160 MHz

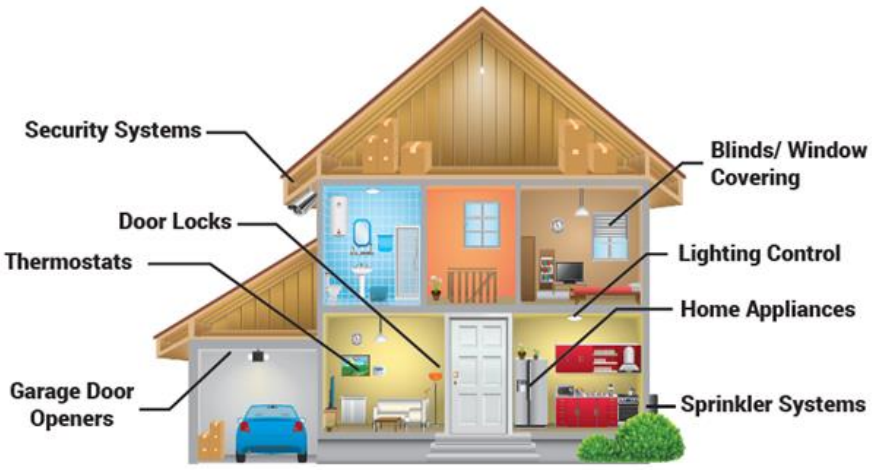
- Hardware accelerators
  - General HW CRC engine
  - HW zeroing function for fast booting
  - Pseudo random number generator (PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provides TCP/IP stack: in the form of network socket APIs
- Advanced security
  - Secure booting
  - Secure debugging using JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES (128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Supports three ultra-low power sleep modes
  - ROM: 256 KB, SRAM: 512 KB, OTP: 8 KB, Retention Memory: 48 KB
- SPI flash Memory
  - 32 M-bit / 4 M-byte
- External Clock source
  - 40 MHz crystal (± 25 ppm) for master clock (initial + temp + aging)
  - 32.768 kHz crystal (± 250 ppm) for RTC clock
- Supply
  - Operating voltage: 2.1 V to 3.6 V (typical: 3.3 V)
  - 2 Digital I/O Supply Voltage: 1.8 V / 3.3 V
  - Black-out and brown-out detector
- Module Dimensions
  - 13.8 mm × 22.1 mm x 3.3 mm, 37 Pins,
- Operating temperature range
  - -40 °C to 85 °C

Applications

DA16200MOD is a full offload SoC for IoT Applications, such as:

- Security systems
- Door locks
- Thermostats
- Garage door openers
- Blinds
- Lighting control
- Sprinkler systems
- Video camera security systems
- Smart appliances
- Video door bell
- Asset tracker

System Diagram



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1 Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
HW	Hardware
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-dropout Regulator
LLI	Linked-List Item
NVIC	Nested Vectored Interrupt Controller
NVRAM	Non-Volatile RAM
PLL	Phase-locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-lane SPI
RTC	Real-time Clock
SAR ADC	Successive Approximation Analog-to-Digital Converter
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
UART	Universal Asynchronous Receivers and Transmitter
XIP	eXecutein Place
TAP	Test Access Port

2 References

[1] ARM Cortex M4 Processor Technical Reference Manual

[2] ITU-T O.150, General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996

[3] Arm® TrustZone® CryptoCell-312, Revision r1p1, Software Integrators Manual

[4] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture

[5] DA16200_SDK_Programmer_Guide.pdf

[6] AMBA AHB bus specification, Rev 3.0 https://developer.arm.com/documentation/ihi0033/bb

3 Block Diagram

Figure 2 shows the DA16200MOD hardware (HW) block diagram.

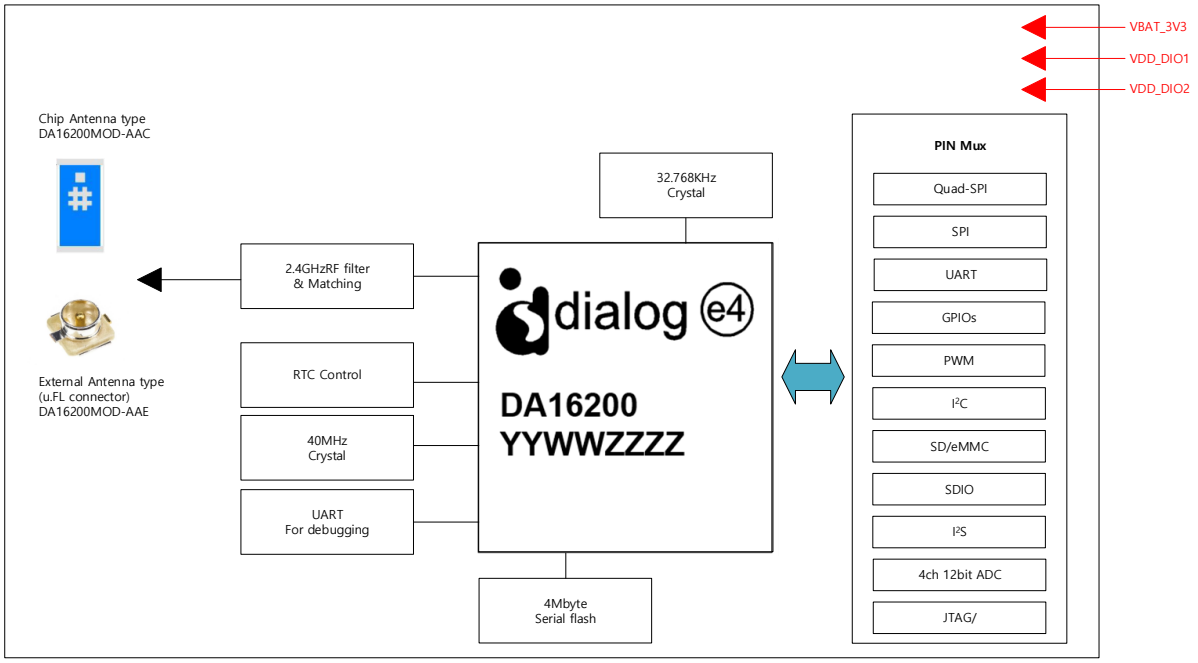

Figure 2: Hardware Block Diagram

Figure 3 shows the DA16200 SoC software (SW) block diagram.

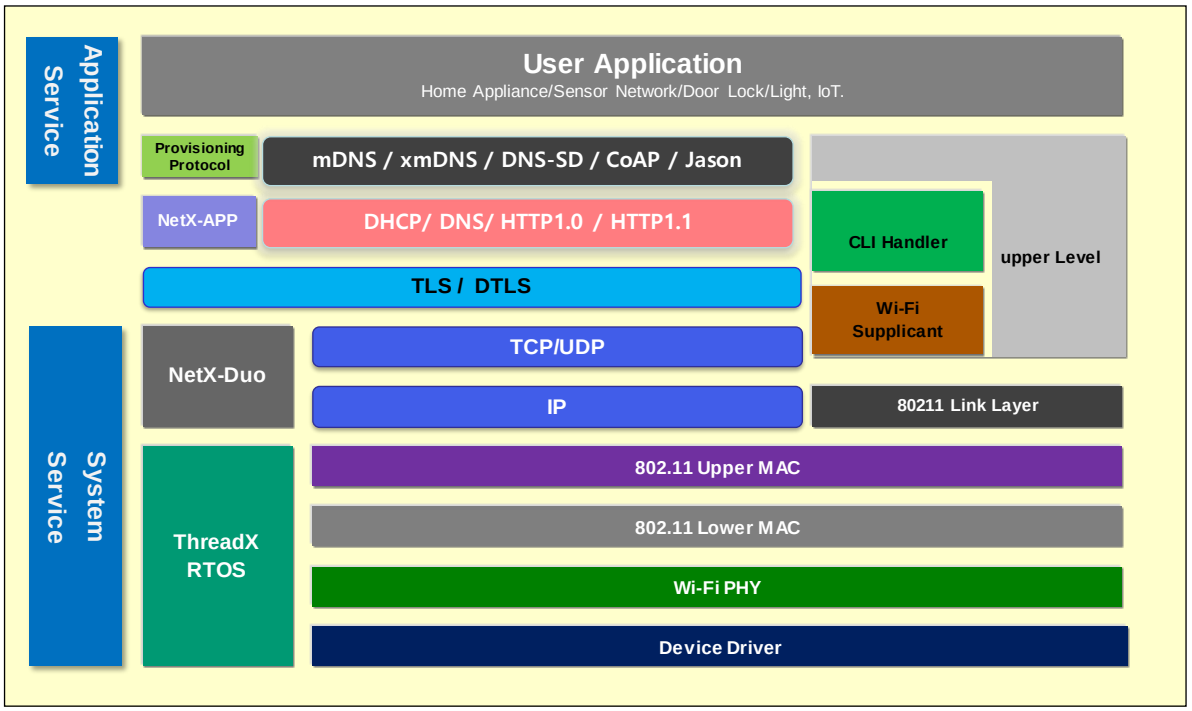

Figure 3: Software Block Diagram

The following descriptions are about the SW block diagrams.

- Kernel layer
  - Real Time Operating System
- The Wi-Fi layer is divided into four layers:
  - Lower MAC
    - SW module to control/handle HW Wi-Fi MAC/PHY and interfaces with Upper MAC layer
  - Upper MAC
    - SW module to control/handle Wi-Fi control/handle to interface with supplicant
    - Wi-Fi Link Layer: Interface layer between Upper MAC and supplicant
    - Supplicant: SW module to control/management to operate Wi-Fi operation
  - Network subsystem layer
    - Used to control/handle network operation
    - Main protocols are IP, TCP, and UDP
    - Other necessary protocols are supported
  - Security Layer
    - Crypto operation engine is ported to use crypto HW engine
- TLS/TCP and DTLS/UDP APIs are supported to handle security operation:
  - User application layer
    - Variable sample codes are supported in SDK – sample codes use supported APIs
    - TCP Client/Server, UDP Client/Server, TLS Client/Server
    - HTTP/HTTPs download, OTA Update usage, and MQTT usage

Customer applications can be included and implemented easily in SDK

4 Pinout

4.1 Pin-out Description (37 pins)

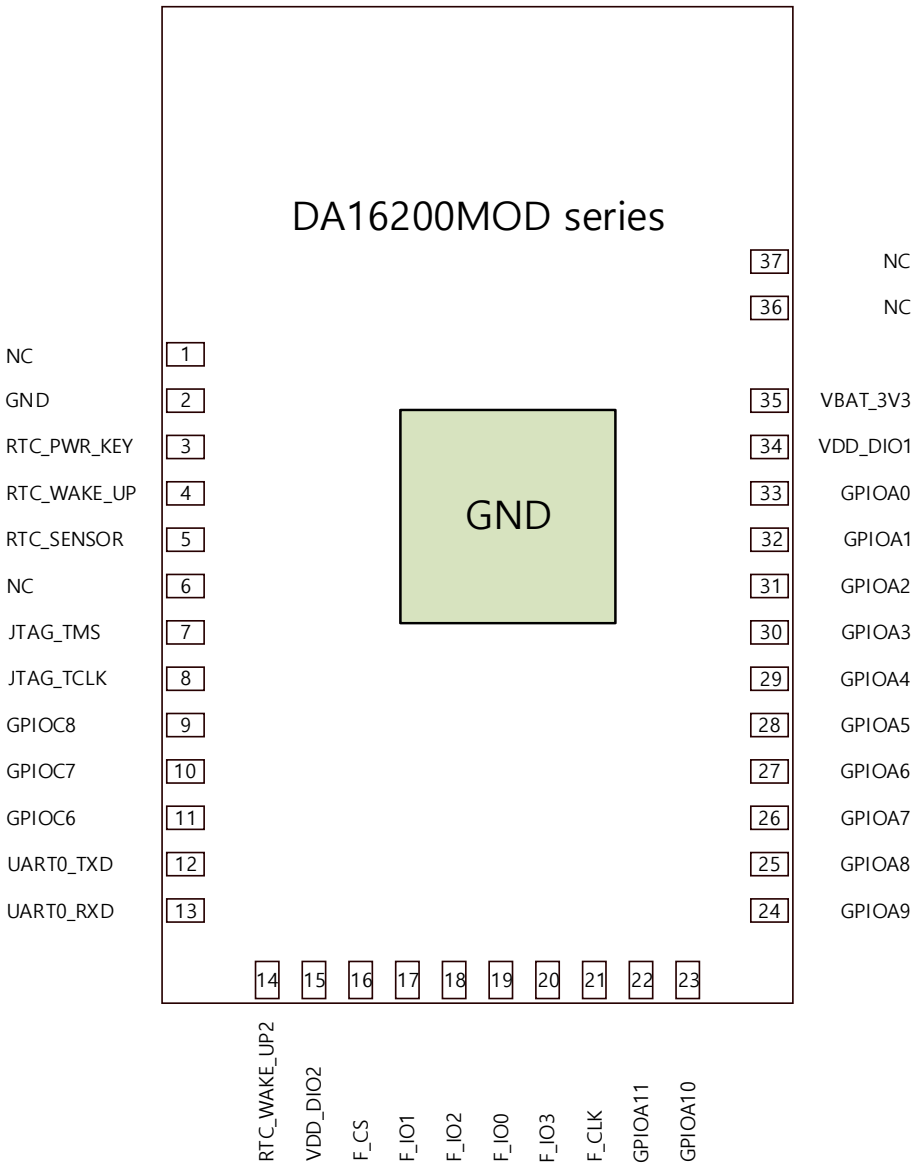

Figure 4: DA16200MOD 37 pins Pin-out Diagram (Top View)

Table 1: Pin Description

#Pin	Pin Name	Type	Drive(mA)	Reset State	Description
1	NC	NC			NOT CONNECT
2	GND	GND			RF VDD
3	RTC_PWR_KEY	DI			RTC block enable signal
4	RTC_WAKE_UP	DI			RTC block wake-up signal
5	RTC_SENSOR	DO			Sensor control signal
6	NC	NC			NOT CONNECT
7	JTAG_TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
8	JTAG_TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
9	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
10	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
12	UART_TXD	DO	2/4/8/12	O	UART transmit data
13	UART_RXD	DI	2/4/8/12	I	UART receive data
14	RTC_WAKE_UP2	DI			RTC block wake-up signal
15	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
16	F_CSN	DIO			External Flash Memory I/F
17	F_IO1	DIO			External Flash Memory I/F (F_SI)
18	F_IO2	DIO			External Flash Memory I/F (F_WP)
19	F_IO0	DIO			External Flash Memory I/F (F_SO)
20	F_IO3	DIO			External Flash Memory I/F (F_HOLD)
21	F_CLK	DIO			External Flash Memory I/F
22	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
23	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
24	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
25	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
26	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
27	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
28	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
29	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
30	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
31	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
32	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
33	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
34	VDD_DIO1	VDD			Supply power for digital I/O
35	VBAT_3V3	VDD			Supply power for integrated power amplifier
36	NC	NC			NOT CONNECT
37	NC	NC			NOT CONNECT

4.2 Pin Multiplexing

This device provides various interfaces to support many kinds of applications. It is possible to control each pin according to the required application in reference to the pin multiplexing illustrated in Table 2. Pin control can be realized through register setting. This device can use a maximum of 16 GPIO pins and each of the GPIO pins multiplexes signals of various functions. In particular, four pins from GPIOA0 to GPIOA3 multiplex analog signals, which also can be realized through register setting.

Table 2: DA16200MOD Pin Multiplexing

Pin	Module default	JTAG	Analog	SPI master	SPI slave	I2C master	I2C slave	SDIO slave	SDeMMC	BT coex	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin State (nRESET=0)	Driving Strength (Note 1)
GPIOA0	GPIO		CH0		SPI_MISO	I2C_SDA	I2C_SDA				BCLK		TXD		Yes	I-PD	2/4/8/12mA
GPIOA1	GPIO		CH1		SPI_MOSI	I2C_CLK	I2C_CLK		WRP		MCLK		RXD		Yes	I-PD	2/4/8/12mA
GPIOA2	GPIO		CH2		SPI_CSB		I2C_SDA				SDO		TXD		Yes	I-PD	2/4/8/12mA
GPIOA3	GPIO		CH3		SPI_CLK		I2C_CLK				LRCK	CLK_IN	RXD		Yes	I-PD	2/4/8/12mA
GPIOA4	UART1_TXD					I2C_SDA	I2C_SDA	CMD	CMD		BCLK		TXD/RTS		No	I-PD	2/4/8/12mA
GPIOA5	UART1_RXD					I2C_CLK	I2C_CLK	CLK	CLK		MCLK		RXD/CTS		No	I-PD	2/4/8/12mA
GPIOA6	WPS			SPI_CSB	SPI_CSB		I2C_SDA	D3	D3		SDO		TXD		No	I-PD	2/4/8/12mA
GPIOA7	Factory_reset			SPI_CLK	SPI_CLK		I2C_CLK	D2	D2		LRCK		RXD		No	I-PD	2/4/8/12mA
GPIOA8	GPIO			SPI_DIO0	SPI_MISO	I2C_SDA		D1	D1	BT_SIG0	BCLK				No	I-PD	2/4/8/12mA
GPIOA9	GPIO			SPI_DIO1	SPI_MOSI	I2C_CLK		D0	D0	BT_SIG1	MCLK				No	I-PD	2/4/8/12mA
GPIOA10	GPIO			SPI_DIO2	SPI_MISO				WRP	BT_SIG2		CLK_IN		TXD	No	I-PD	2/4/8/12mA
GPIOA11	GPIO			SPI_DIO3	SPI_MOSI									RXD	No	I-PD	2/4/8/12mA
TCLK/ GPIOA15	TCLK	TCLK													No	I-PD	2/4/8/12mA
TMS	TMS	TMS													No	I-PU	2/4/8/12mA
UART_TXD	UART0_TXD														No	O	2/4/8/12mA
UART_RXD	UART0_RXD														No	I	2/4/8/12mA
GPIOC8	GPIO	TDI													No	I-PD	2/4/8/12mA
GPIOC7	GPIO	TDO												RXD	No	I-PD	2/4/8/12mA
GPIOC6	GPIO	NTRST												TXD	No	I-PD	2/4/8/12mA

Note 1 Default Value: 8 mA

5 Electrical Specification

5.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Pins	Min	Max	Units
VBAT_3V3	35	VSS	3.9	V
VDD_DIO1	34	VSS	3.9	V
VDD_DIO2	15	VSS	3.9	V
Operating temperature range (TA)		-40	+85	°C

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Pins	Min	Typ	Max	Units
VBAT_3V3	35	2.1		3.6	V
VDD_DIO1	34	1.62		3.6	V
VDD_DIO2	15	1.62		3.6	V
Operating temperature range (TA)		-40		+85	°C

5.3 Electrical Characteristics

5.3.1 DC Parameters, 1.8 V IO

Table 5: DC Parameters, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic High level	0.7 × DVDD		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.2 × DVDD	V
Output High Voltage	V_{OH}	DVDD=Min.	0.8 × DVDD		DVDD	V
Pull-up Resistor	R_{PU}	$V_{PAD}=V_{IH}$, DIO=Min.			32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=VIL, DIO=Min.			32.4	

Note 1 DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level

5.3.2 DC Parameters, 3.3 V IO

Table 6: DC Parameters, 3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.8	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.0		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.4	V
Output High Voltage	V_{OH}	DVDD=Min.	2.4		DVDD	V
Pull-up Resistor	R_{PU}	VPAD=VIH, DIO=Min.			19.4	kΩ
Pull-down Resistor	R_{PD}	$V_{PAD}=V_{IL}$, DIO=Min.			16.0	

Note 1 DVDD= 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level

5.3.3 DC Parameters for RTC Block

There are several control pins in RTC block, see Section 7.3 RTC for detail.

Table 7: DC Parameters for RTC block, 3.3 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.6	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.2		VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

Table 8: DC Parameters for RTC block, 2.1 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.6		VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

5.3.4 DC Parameters for Digital Wake-up

Several GPIOs can be used for wake-up, see Section 7.3.1 Wake-up Controller for detail.

To use Digital Wake-up, IO voltage should not be over VBAT.

Table 9: DC Parameters for Digital Wake-up, 3.3 V VBAT & 1.8/3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.5	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.4		DVDD	V

(DVDD= 1.8/3.3V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be over VBAT)

Table 10: DC Parameters for Digital Wake-up, 2.1 V VBAT & 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.3	V
Input High Voltage	V_{IH}	Guaranteed logic High level	1.3		DVDD	V

(DVDD= 1.8V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be over VBAT)

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

TA = +25 °C, VBAT = 3.3 V, CH1(2412 MHz)

Table 11: WLAN Receiver Characteristics

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	1 Mbps DSSS	-99.5	-98.5	-96.5	dBm
	2 Mbps DSSS	-95	-94	-92	
	11 Mbps CCK	-90	-89	-87	
	6 Mbps OFDM	-91	-90	-88	
	9 Mbps OFDM	-91	-90	-88	
	18 Mbps OFDM	-89	-88	-86	
	36 Mbps OFDM	-82	-81	-79	
	54 Mbps OFDM	-76	-75	-73	
	MCS0(GF)	-91	-90	-88	
	MCS7(GF)	-73	-72	-70	
Maximum input level (8 % PER for 11b rates, 10 % PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

5.4.2 WLAN Transceiver Characteristics

TA = +25 °C, VBAT = 3.3 V, CH1(2412 MHz)

Table 12: WLAN Transmitter Characteristics

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	16.5	19.0	20	dBm
	2 Mbps DSSS	16.5	19.0	20	
	5.5 Mbps CCK	16.5	19.0	20	
	11 Mbps CCK	16.5	19.0	20	
	6 Mbps OFDM	15.5	18.0	19	
	9 Mbps OFDM	15.5	18.0	19	
	12 Mbps OFDM	15.5	18.0	19	
	18 Mbps OFDM	15.5	18.0	19	
	24 Mbps OFDM	14.5	17.0	18	

Parameter	Condition	Min	Typ	Max	Units
	36 Mbps OFDM	14.5	17.0	18	
	48 Mbps OFDM	13	15.5	16.5	
	54 Mbps OFDM	12	14.5	15.5	
	MCS0 OFDM	15.5	18.0	19	
	MCS7 OFDM	12	14.5	15.5	
Transmit center frequency accuracy		-25		+25	ppm

5.5 Current Consumption

TA = +25 °C, VBAT = 3.3 V, w/ CPU clock is 80 MHz.

Table 13: Current Consumption in Active State

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 19.0 dBm	260	280	320	mA
		6 Mbps OFDM	@ 18.0 dBm	240	260	300	
		54 Mbps OFDM	@ 14.5 dBm	180	200	240	
		MCS7	@ 14.5 dBm	180	200	240	
	RX	No signal (Note 1)		25	29	51	
		1 Mbps DSSS (Note 1)		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.5	54	

Note 1 Low Power Mode& CPU clock 30 MHz

TA = +25 °C, VBAT = 3.3 V

Table 14: Current Consumption in Low Power Operation

Parameter	Condition	Min	Typ	Max	Units
Low Power Operation	Sleep 1		0.2		µA
	Sleep 2		1.8		
	Sleep 3		3.5		

5.6 Radiation Performance

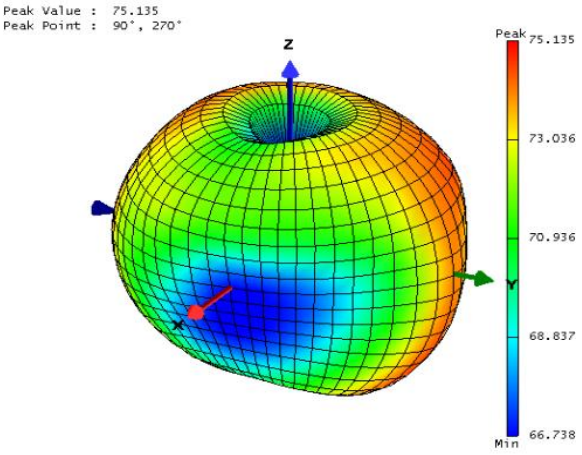

Figure 5: TIS 3D

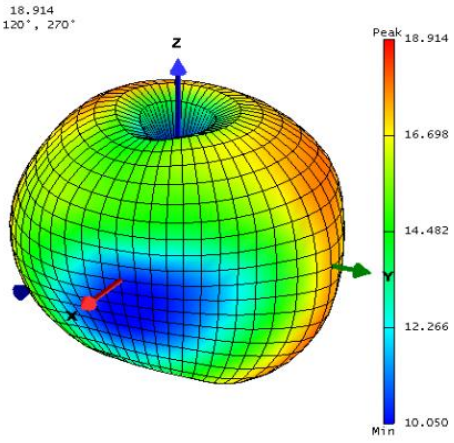

Figure 6: TRP 3D

5.7 ESD Ratings

Table 15: ESD Performance

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001-2017	± 2,000 V	Pass
Charge Device Mode (CDM)	ANSI/ESDA/JEDEC JS-002-2018	± 500 V	Pass

5.8 Clock Electrical Characteristics

DA16200MOD is including two clock sources. One is the 32.768 kHz clock used by the RTC block, and the other is the 40 MHz clock for the internal processor and Wi-Fi system. More specifically, the 40 MHz clock is used as a source clock for the internal PLL while the PLL output is used for the internal processor and Wi-Fi system block.

5.8.1 RTC Clock Source

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The RTC block of the SoC contains an internal 32.768 kHz RC oscillator as well, which is used as a clock for chip initialization before the external 32.768 kHz crystal reaches the stable time in the initial stage. It is necessary to convert it into an external clock for accurate clock counting after the initialization stage. This process is executed through the register setting.

5.8.2 Main Clock Source

DA16200MOD contains a crystal oscillator for the main clock source which supports the external crystal clock. Basically, the external clock is 40 MHz.

6 Power Management

DA16200MOD has an RTC block which provides power management and function control for low power operation. In normal operation, the RTC block is always powered on when RTC_PWR_KEY is enabled.

6.1 Power On Sequence

The sequence after the initial switching from power-off to power-on is shown in Figure 7.

The RTC_PWR_KEY of DA16200 is a pin that enables the RTC block. Once RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are switched on automatically in the sequence pre-defined by the RTC block.

Once RTC_PWR_KEY is switched on, LDOs for both XTAL and digital I/O are switched on shortly and then the DC-DC regulator is switched on according to the pre-defined interval. The enabling intervals can also be modified in the register settings after initial power-up.

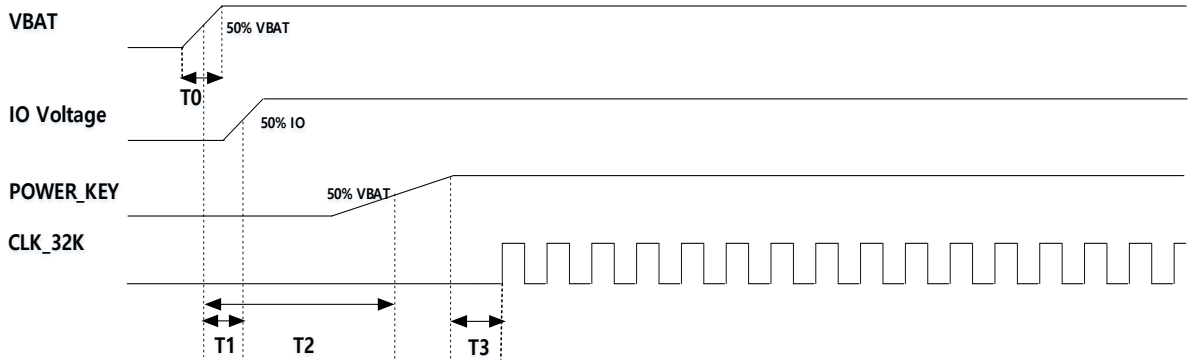

Figure 7: Power on Sequence

Table 16: Power on Sequence Timing Requirements

Name	Description	Min	Typ	Max	Unit
T0	VBAT power-on time from 10 % to 90% of VBAT				ms
T1	IO voltage and VCC supply		0		ms
T2	RTC_PWR_KEY switch-on time from 50 % VBAT to 50 % POWER_KEY * Note 1		5*T0		ms
T3	Internal RC oscillator wake-up time		217		µs

Note 1 If the T0 = 10 ms to switch on VBAT, the recommended T2 is 50 ms for the safe booting operation. It would be externally controlled by MCU or it would be implemented using RC filter at the input of RTC_PWR_KEY. The recommended C is 470 nF or 1uF (not to exceed 1 uF) and R value is chosen to have T2 delay. For example, R and C values will be 82 kΩ and 1 uF when T0 = 10 ms.

6.2 Low Power Operation Mode

DA16200MOD provides three Sleep modes as low power operation modes.

6.2.1 Sleep Mode 1

Sleep mode 1 is an operational mode in which the RTC_PWR_KEY is not switched to high yet. The RTC_PWR_KEY is in the low state and the DA16200MOD is only supplied with VBAT power. With all the internal blocks off in Sleep mode 1, only the leakage current from a minimal number of internal blocks connected to VBAT remains.

6.2.2 Sleep Mode 2

Sleep mode 2 is an operational mode in which the RTC_PWR_KEY is set to high and the RTC block is running. Sleep mode 2 is activated by setting RTC registers for controlling the power management unit via a command from the CPU.

To switch Sleep mode 2 back to Sleep mode 1, RTC_PWR_KEY should be set to low.

Changing the state of the device from Sleep mode 2 to an ACTIVE state happens in one of two ways:

1. The counter value that has been set by the CPU prior to entering Sleep mode 2 is reached.
2. An external wake-up event occurs via the RTC_WAKE_UP pin.

6.2.3 Sleep Mode 3

Sleep Mode 3 is a low power, but fully connected Wi-Fi mode of operation. Sleep Mode 3 checks for incoming Wi-Fi network data traffic at regular intervals set by the user, for example, every one second, three seconds, five seconds, and so on. The exact time interval is programmable.
Sleep Mode 3 is activated by software commands. See the SDK documentation for more information.
A device can come out of Sleep Mode 3 and into a fully ACTIVE state before the next targeted wakeup time interval via a GPIO wakeup.

7 Core System

7.1 ARM Cortex-M4F Processor

The Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, low-cost debug, and includes floating point arithmetic functionality. The processor is intended for deeply embedded applications that require fast interrupt response features.

The features of the Cortex-M4F processor in DA16200 are summarized below:

- Operation clock frequency is up to 160 MHz
- 32-bit ARM Cortex-M4F architecture optimized for embedded applications
- Thumb-2 mixed 16/32-bit instruction set
- Hardware division and fast multiplication
- Includes Nested Vectored Interrupt Controller (NVIC)
- SysTick timer provided by Cortex-M4F processor
- Supports both standard JTAG (5-wire) and the low-pin-count ARM SWD (2-wire, TCLK/TMS) debug interfaces
- Cortex-M4F is binary compatible with Cortex-M3

For more information on the ARM Cortex-M4F, see the *ARM Cortex-M4F r0p1 technical reference manual* **Error! Reference source not found.**.

7.2 Wi-Fi Processor

DA16200 includes an internal MCU (ARM Cortex-M4F) to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast and secure WLAN and Internet connections with 256-bit encryption. It supports the station, SoftAP, and Wi-Fi Direct modes. It also supports WPA/WPA2 personal and enterprise security, WPA2 SI, WPA3 SAE, OWE, and WPS 2.0. It includes an embedded IPv4 and IPv6 TCP/IP stack.

7.3 RTC

Among the pins in DA16200MOD, four special pins are directly connected to the RTC block, which are RTC_PWR_KEY, RTC_GPO, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 17: RTC Pin Description

Pin Name	Pin Number	Description
RTC_PWR_KEY	3	RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a pre-defined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in DA16200. When disabled, all blocks are powered off and this mode is defined as Sleep mode 1. Minimum leakage current in Sleep mode 1.
RTC_SENSOR	5	This pin is an output and high level is 'VBAT'. It has three different functions. ● GPO function: output value can be set as 1 or 0 via register setting. It can keep the value even in Sleep mode ● Flash control function: when in Sleep mode, it becomes 0; when in Active mode, it is 1 ● Sensor wakeup function: when used in sensor wake-up function (Section 8.8.4), it provides a programmable periodic signal for an external device. Inside the RTC, there are registers for setting count values

Pin Name	Pin Number	Description
RTC_WAKE_UP	4	This pin is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal via this pin and wakes up DA16200 from Sleep mode 2 or Sleep mode 3.
RTC_WAKE_UP2	14	

RTC block has a 36-bit real time counter. Its resolution is equal to one clock period of 32.768 kHz. The count value can be read via the register read command.

7.3.1 Wake-up Controller

The wake-up controller is designed to wake up DA16200MOD from a Sleep mode by an external signal. It detects an edge trigger of the wake-up signal and selects either the rising edge or the falling edge. Also, the wake-up signal must be maintained for at least 200 µs upon occurrence of transition on one side.

When it comes to the source of wake-up, 11 digital I/Os in addition to the two pins directly connected to the RTC block can be used. Although up to 11 digital I/Os are available for use, the maximum number of digital I/Os that are simultaneously available is eight. Table 18 describes the digital I/Os that are available for simultaneous use.

Table 18: Wake-up Sources

Input Selection = 0	Input Selection = 1
GPIOA4	X
GPIOA5	X
GPIOA6	X
GPIOA7	X
GPIOA8	X
GPIOA9	GPIOC6
GPIOA10	GPIOC7
GPIOA11	GPIOC8

For more on wake-up source selection, refer to input selection register: 0x50091008[25:16].

The wake-up controller is located in the RTC block. Several parameters can be set by RTC registers and they identify which pin is used to wake up the SoC by checking the status register after wake-up.

DA16200MOD has another wake-up function using analog sources, which is described in Section 8.8.4. Using the Aux-ADC, DA16200 detects whether it exceeds the pre-defined threshold value. If it detects the wanted condition, it will wake up from a Sleep mode. Four ports (GPIOA[3:0]) are used for this function.

7.3.2 Retention I/O Function

DA16200MOD I/O has a retention mode. During this mode, I/O cells retain the previous state values at the core side inputs. When it is required to maintain the value of a specific GPIO in Sleep mode, this function will be used. For example, in order to maintain HIGH value on GPIOA4 in Sleep mode, it is required to set the value of GPIOA4 to HIGH and set the register bit of RTC block (0x5009_1018:BIT[27:24]) to enable retention to the proper value described in Table 19 before going to the Sleep mode. For GPIOA4, BIT[25] should be set to HIGH, then GPIOA4 can keep the value HIGH during the Sleep mode.

The retention enable register is comprised of three bits in total, and the I/O power domains covered by each of the bits are described in Table 19.

Table 19: I/O Power Domain

[25] DIO1	[26] DIO2	[27] FDIO
GPIOA[11:4]	GPIOC[8:6]	F_CLK
	TCLK/TMS	F_CSN
	UART0_RXD/UART0_TXD	F_IO0 to F_IO3

7.4 Pulse Counter

7.4.1 Introduction

The pulse counter is a module which counts the number of rising or falling edges of input signals. And this counter module can run even in Sleep mode. It includes one 32-bit up-counter. The input channel can be chosen by register setting among the 11 digital I/Os. It also has a glitch filter which is designed to remove the unwanted trigger of an input signal.

7.4.2 Functional Description

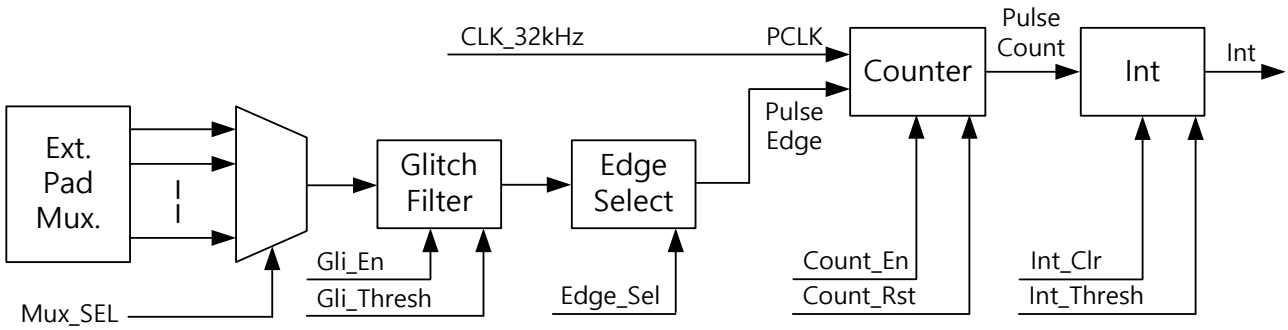

Figure 8: Pulse Counter Block Diagram

7.4.2.1 Input

Available input channels are described in Table 18. It uses the same input sources with the wake-up controller. By register setting, input channels can be selected among 11 digital I/Os.

7.4.2.2 Clock

The operation clock of the pulse counter is 32 kHz.

7.4.2.3 Counter

As described in Figure 8, the pulse counter is activated by several counter control signals. By register setting, input signals can be selected on either the rising edges or falling edges. In order to enable the glitch filter module, Gli_En and Gli_Thresh register values need to be set. The pulses whose cycles are shorter than the Gli_Thresh value are removed. The counter is a 32-bit up-counter and the counter value can be reset to zero by Count_Rst.

7.4.2.4 Interrupts

An interrupt occurs when the counter values reaches the Interrupt Threshold value (Int_Thresh). In Sleep mode, this interrupt can be used as a wake-up source.

8 Peripherals

This section describes the peripherals that are supported by the DA16200MOD.

8.1 QSPI: Master with XIP Feature

QSPI master supports 4-line SPI communication with commercial flash memory devices and uses Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when the 1-line communication mode is used, it can be used as the SPI master.

QSPI master is an IP for communication between the flash memory and AMBA AHB bus and is designed to support XIP. The features of the QSPI master are summarized as follows:

Serial Flash Interface:

- SPI compatible serial bus interface
  - Configurable SPI I/O modes:
    - Single I/O mode
    - Dual I/O mode
    - Quad I/O mode
  - JEDEC Standard: JESD216B
  - 24-bit and 32-bit addressing
  - Supports to access flash with XIP mode
    - Read access without command
    - Read access without address and command
  - Programmable SPI clock phase and polarity
  - Maximum number of SPI CS is four that can be operated

AMBA Slave Interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [6]
- Direct code execution: directly addressable access without additional driver software
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction
- AMBA slave interface is optional to access configuration and status registers
- Simple timer is used to check the completion time of flash operation
- XIP path of QSPI master supports HW remapping function to execute selected boot image for over-the-air programming (OTA)

AMBA Master Interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [6]
- Supports DMA operation to access serial flash devices
  - Automatic copy of code image from serial flash to system RAM
  - Automatic programming of code image from system RAM to serial flash
- Performs a mem-to-mem copy in units of 32 bits, regardless of the address and length
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction

Figure 9 shows the QSPI Master Block Diagram.

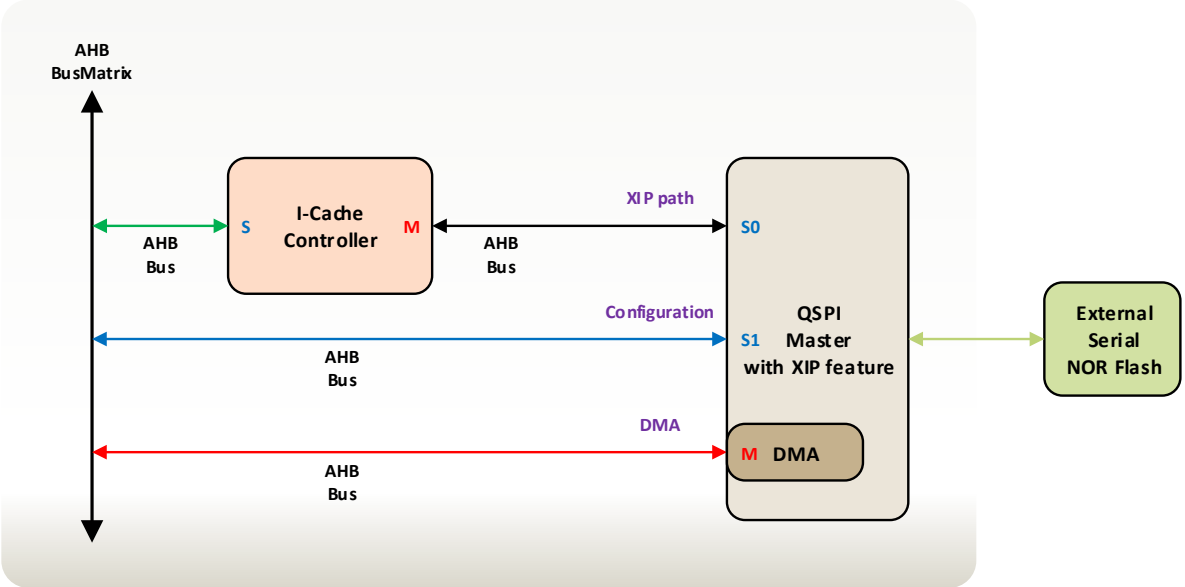

Figure 9: QSPI Master Block Diagram

Figure 10 shows the timing diagram for the QSPI master.

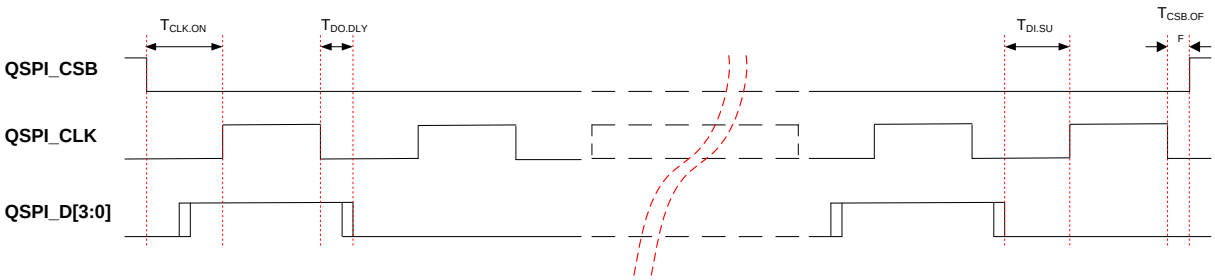

Figure 10: QSPI Master Timing Diagram (Mode 0)

Table 20 lists the timing parameters for the QSPI master.

Table 20: QSPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	10		120	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 ×T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

8.2 SPI Master

QSPI can use the SPI master by means of single line interface. Table 21 shows the pin definition of the SPI master interface. SPI signal timing is the same as QSPI.

To use DA16200MOD as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from GPIO special function by setting the registers in the GPIO.

Table 21: SPI Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOx		O	E_SPI_CSB[3:1]
GPIOA6	27	O	E_SPI_CSB[0]
GPIOA7	26	O	E_SPI_CLK
GPIOA8	25	I/O	E_SPI_MOSI or E_SPI_D[0]
GPIOA9	24	I/O	E_SPI_MISO or E_SPI_D[1]
GPIOA10	23	I/O	E_SPI_D[2]
GPIOA11	22	I/O	E_SPI_D[3]

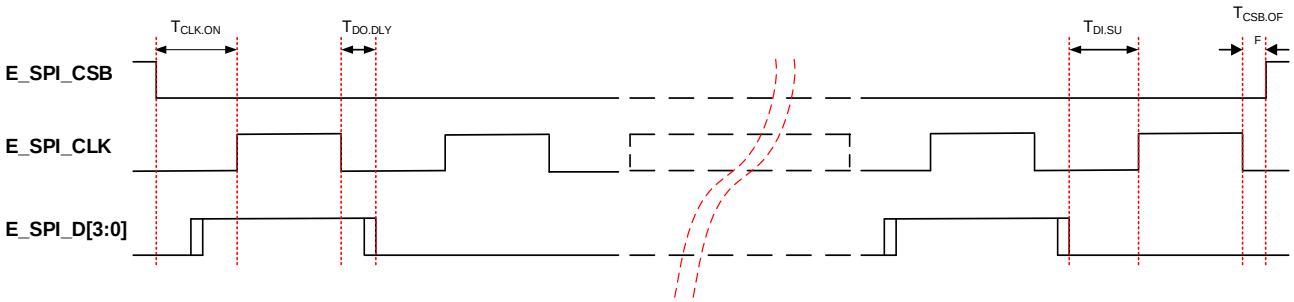

Figure 11: SPI Master Timing Diagram (Mode 0)

Table 22: SPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	5		60	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 × T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

8.3 SPI Slave

SPI slave interface supports the control of DA16200 by an external host. The range of SPI clock speed is the same as that of the internal bus clock speed. The SPI slave supports both the burst mode and non-burst mode. In the burst mode, SPI_CSB remains active from the start to the end of communication. In the non-burst mode, SPI_CLK remains active at every eight bits.

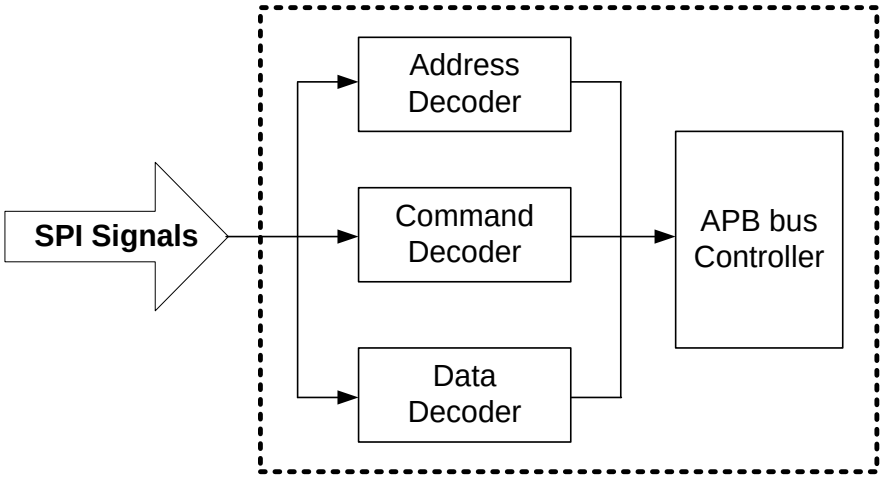

Figure 12: SPI Slave Block Diagram

Communication protocols of the SPI slave interface use either 4-byte or 8-byte control signals. Between the two available communication protocols, the CPU chooses one before initiating the control.

Figure 13 and Figure 14 shows the 8-byte and 4-byte control types.

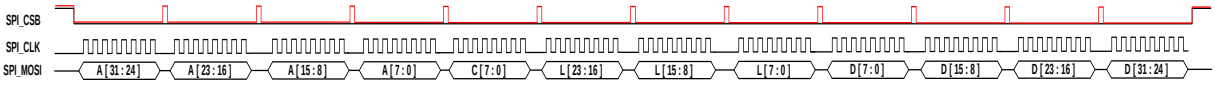

Figure 13: 8-byte Control Type

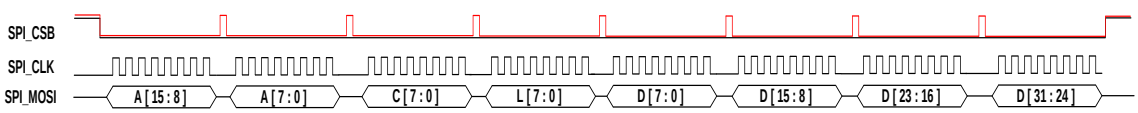

Figure 14: 4-byte Control Type

The 8-byte control type uses 4-byte address, 1-byte control, and 3-byte length. The 4-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 3-byte length shows the length of data subject to continuous access in bytes. Hence, when the 8-byte control type is applied, the maximal length of data subject to continuous access is 16 MB.

The 4-byte control type uses 2-byte address, 1-byte control, and 1-byte length. The 2-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 1-byte length shows the length of data subject to continuous access in bytes. Since the 32-bit address map is used internally, the 2-byte address is not enough to express everything. Thus, the upper 2-byte base address is designated, and then the lower 2-byte address is used.

Table 23 and Table 24 shows the meaning of each bit in the 1-byte control in the 8-byte control type and the 4-byte control type, respectively.

Table 23: Control Field of the 8-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal Address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5:0		Not used. Set all bits to ‘0’	

Table 24: Control Field of the 4-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5	Common	1 = Refer base address as common area	0 = Refer base address
4	Length section	1 = Refer to register value	0 = Refer to length field
3:0	Length[12:8]	Length field upper	

Table 25 shows the pin definition of the SPI slave interface.

Table 25: SPI Slave Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA2	31	I	SPI_CSB
GPIOA6	27	I	
GPIOA3	30	I	SPI_CLK
GPIOA7	26	I	
GPIOA1	32	I	SPI_MOSI
GPIOA9	24	I	
GPIOA11	22	I	
GPIOA0	33	O	SPI_MISO
GPIOA8	25	O	
GPIOA10	23	O	

Figure 15 shows the timing diagram for the SPI slave.

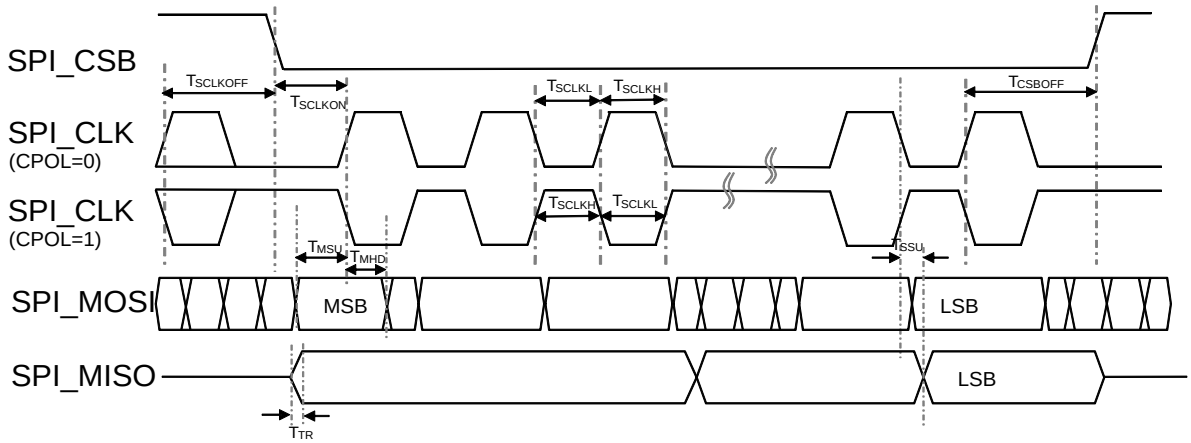

Figure 15: SPI Slave Timing Diagram

Table 26 lists the timing parameters for the SPI slave.

Table 26: SPI Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}	-	-	50	MHz
SCLK clock duty		40			%
Non active duration	$T_{SCLKOFF}$	400	-	-	ns
1st CLK active rising transition time	T_{SCLKON}	T_{SCLKL}(CPOL=0) T_{SCLKH} (CPOL=1)	-	-	ns
CSB non active rising transition time	T_{CSBOFF}	T_{SCLKH} (CPOL=0) T_{SCLKL} (CPOL=1)	-	-	ns
MOSI setup time	T_{MSU}	8	-	T_{SCLK} (Note 1)	ns
MOSI hold time	T_{MHD}	8	-	T_{SCLK}	ns
MISO delay time	T_{SSU}	-	-	8	ns
MISO transition time(10% to 90% transition)	T_{TR}	-	4	5	ns

Note 1 $T_{SCLK} = 0.5 \times (F_{SCLK} \times 10^{6})^{-1}$ second

8.4 SDIO

SDIO is a full/high speed card suitable for memory card and I/O card applications with low power consumption. The full/high speed card supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 50 MHz. To be compatible with the serviceable SDIO clock, the internal BUS clock needs to be set to minimum 50 MHz. The CIS and CSA area is located inside the internal memory and the SDIO registers(CCCR and FBR) are programmed by the SD host.

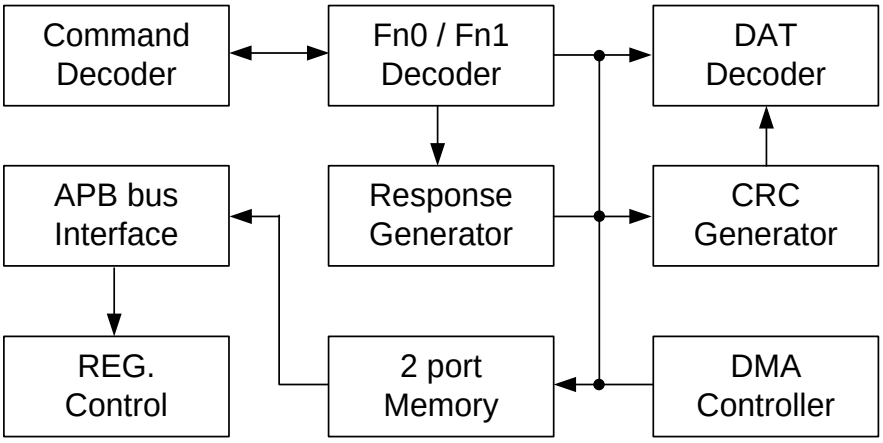

Figure 16: SDIO Slave Block Diagram

Table 27 shows the pin definition of the SDIO interface.

The GPIOA4 and GPIOA5 pins are set to SDIO CMD and CLK by default. If SDIO initialization is performed and SDIO communication is enabled, SDIO data pin setting is performed automatically. In other words, when the SDIO communication is detected, the pin used as the SDIO data among the GPIO pins is automatically activated in the SDIO use mode. However, the auto setting function is not supported for the F_xxx pin used as the flash function.

Table 27: SDIO Slave Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA4	29	I/O	SDIO_CMD
GPIOA5	28	I	SDIO_CLK
GPIOA9	24	I/O	SDIO_D0
GPIOA8	25	I/O	SDIO_D1
GPIOA7	26	I/O	SDIO_D2
GPIOA6	27	I/O	SDIO_D3

Figure 17 shows the timing diagram for the SDIO slave.

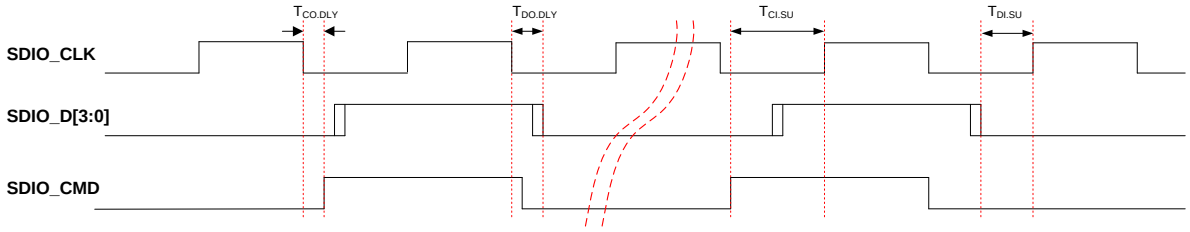

Figure 17: SDIO Slave Timing Diagram

Table 28 lists the timing parameters for the SDIO slave.

Table 28: SDIO Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CLK frequency	F_{SCLK}	-	-	50	MHz
SDIO_CLK clock duty			50		%
SDIO_CMD input setup time	$T_{CI.SU}$	3			ns

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CMD output delay time	$T_{CO.DLY}$			11 (Note 1)	ns
SDIO_D[3:0] input setup time	$T_{DI.SU}$	3			ns
SDIO_D[3:0] output delay time	$T_{DO.DLY}$			11 (Note 1)	ns

Note 1 SDIO signals can set previous output from half cycle.

8.5 I2C Interface

8.5.1 I2C Master

DA16200MOD includes an I2C master module. Three ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), and high (1.0 MHz) speed mode. Table 29 shows the pin definition of the I2C master interface.

Table 29: I2C Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	O	I2C_CLK
GPIOA5	28	O	
GPIOA9	24	O	
GPIOA0	33	I/O	I2C_SDA
GPIOA4	29	I/O	
GPIOA8	25	I/O	

Figure 18 shows the I2C timing diagram. The timing diagram is the same as that of I2C slave timing diagram.

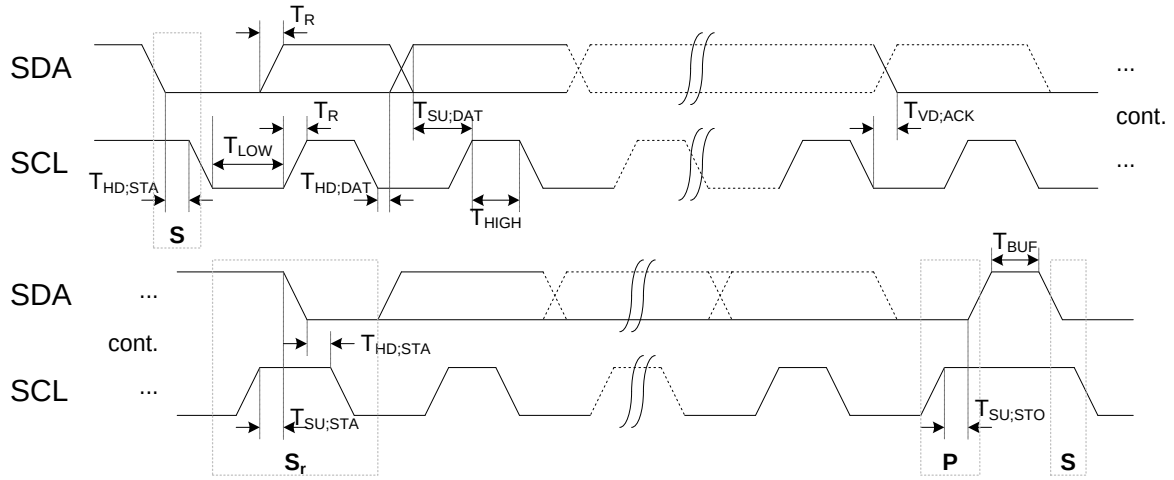

Figure 18: I2C Master Timing Diagram

Table 30 lists the I2C master timing parameters.

Table 30: I2C Master Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
Bus clock frequency	F_{op_clk}	30	160	30	160	MHz

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	100	400	100	1000 (Note 2)	kHz
Clock Duty (Note 1)		40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.2	-	0.2	-	µs
Low period of the SCL clock	T_{LOW}	1.27	-	0.55	-	µs
High period of the SCL clock	T_{HIGH}	1.23	-	0.45	-	µs
Setup time for START condition	$T_{SU;STA}$	1.1	-	0.37	-	µs
Data hold time	$T_{HD;DAT}$	3x T_{op_clk} (Note 4)	-	3x T_{op_clk} (Note 4)	-	µs
Data setup time	$T_{SU;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	µs
Rise time of both SDAand SCL	T_R (Note 3)	0.02	0.3	0.05	0.05	µs
Setup time for STOP condition	$T_{SU;STO}$	0.36	-	0.45	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	3x T_{op_clk} (Note 4)	-	3x T_{op_clk} (Note 4)	-	µs
Buffer free time between START and STOP condition	T_{BUF}	0.5	-	0.5	-	µs

Note 1 Clock duty ratio = (T_{HIGH} /T_{SCLK}) × 100[%], T_{SCLK} = 1/ F_{SCLK}

Note 2 Max. clock = 1.0 MHz (clock period = 1000 ns)

Note 3 T_R depends on a pull-up resistor value.

Note 4 T_{op_clk} = (1 / F_{op_clk}) x 10^6 usec

8.5.2 I2C Slave

I2C slave interface supports the control of DA16200MOD by an external host. Pin mux condition is defined in Table 31. Three ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), and high (1.0 MHz) speed mode.

Table 31: I2C Slave Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	I	I2C_CLK
GPIOA3	30	I	
GPIOA5	28	I	
GPIOA7	26	I	
GPIOA0	33	I/O	I2C_SDA
GPIOA2	31	I/O	
GPIOA4	29	I/O	
GPIOA6	27	I/O	

Figure 19 shows the I2C slave timing diagram.

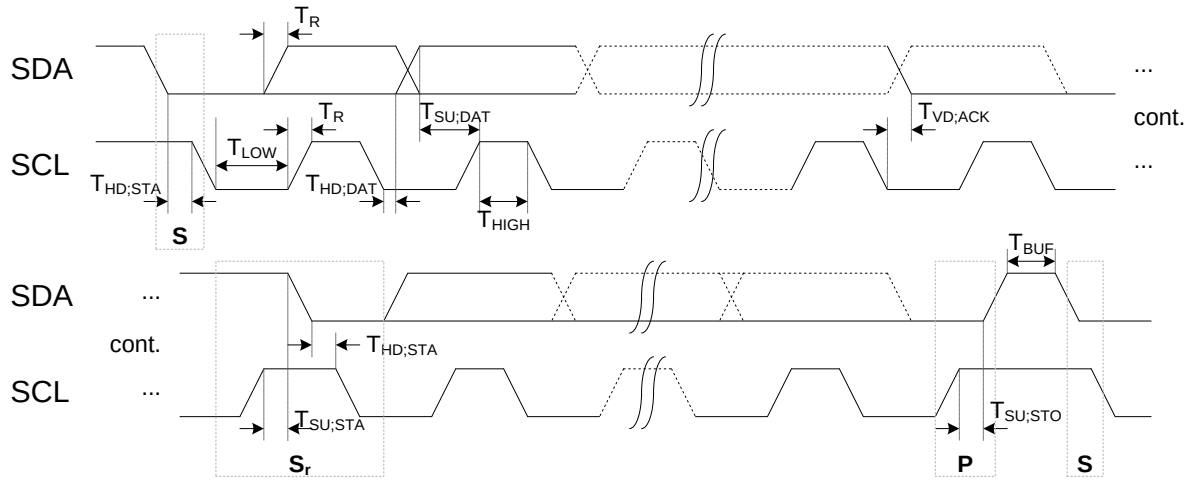

Figure 19: I2C Slave Timing Diagram

Table 32 lists the I2C slave timing parameters.

Table 32: I2C Slave Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	0	400	0	1000 (Note 2)	kHz
Clock Duty (Note 1)		40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.6	-	0.26	-	µs
Low period of the SCL clock	T_{LOW}	1.3	-	0.5	-	µs
High period of the SCL clock	T_{HIGH}	0.6	-	0.26	-	µs
Setup time for START condition	$T_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$T_{HD;DAT}$	0	-	0	-	µs
Data setup time	$T_{SU;DAT}$	100	-	50	-	ns
Rise time of both SDA and SCL	T_R	20	300	-	120	ns
Setup time for STOP condition	$T_{SU;STO}$	0.6	-	0.26	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	-	-	-	-	µs
Buffer free time between START and STOP condition	T_{BUF}	1.3	-	0.5	-	µs

Note 1 Clock duty ratio = (T_{HIGH} /T_{SCLK}) × 100[%], TSCLK = 1/FSCLK

Note 2 Max. clock = 1.0 MHz (clock period = 1000 ns)

8.6 SD/SDeMMC

The SD/eMMC host IP provides the function for DA16200MOD to access SD or eMMC cards. This SD/eMMC host IP only supports a 4-bit data bus and the maximum clock rate is 50 MHz. The maximum data rate is 25 MB/s (200 Mbps) under the 4-bit data bus and 50 MHz clock.

SD/eMMC pin mux condition is defined in Table 33.

Table 33: SD/eMMC Master Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA4	29	I/O	SD/eMMC_CMD
GPIOA5	28	O	SD/eMMC_CLK
GPIOA9	24	I/O	SD/eMMC_D0
GPIOA8	25	I/O	SD/eMMC_D1
GPIOA7	26	I/O	SD/eMMC_D2
GPIOA6	27	I/O	SD/eMMC_D3
GPIOA10	23	I	SD/eMMC_WRP
GPIOA1	32	I	

8.6.1 Block Diagram

Figure 20 shows the block diagram of SD/eMMC host IP and it includes the control register, clock control, command/response pipe, data pipe, and AHB master interface blocks.

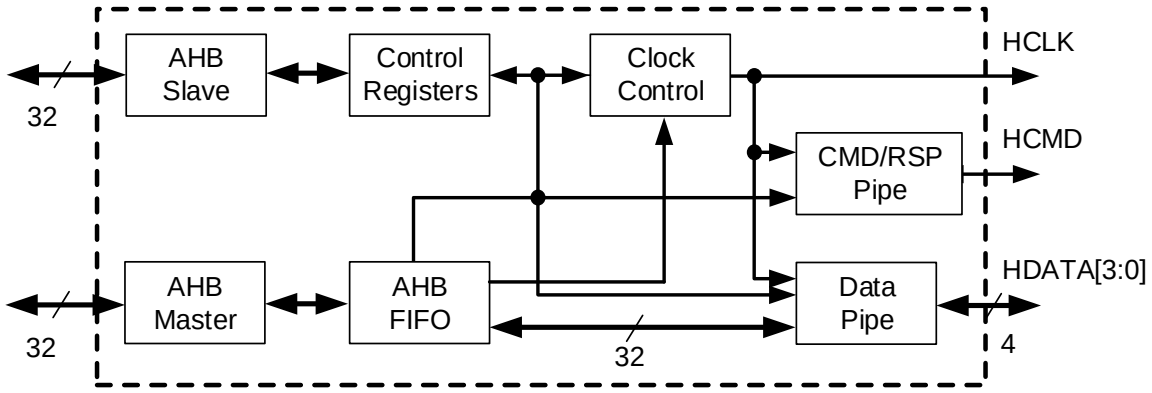

Figure 20: SD/eMMC Block Diagram

Figure 21 shows the timing diagram for the SD/eMMC master.

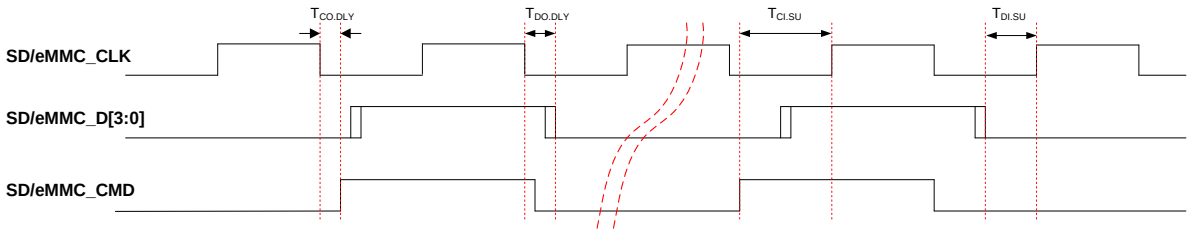

Figure 21: SD/eMMC Master Timing Diagram

Table 34 lists the timing parameters for the SD/eMMC master.

Table 34: SD/eMMC Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SD/eMMC_CLK frequency	F_{SCLK}	-	-	50	MHz
SD/eMMC_CLK clock duty			50		%
SD/eMMC_CMD input setup time	$T_{CI.SU}$	8			ns
SD/eMMC_CMD output delay time	$T_{CO.DLY}$			3	ns
SD/eMMC_D[3:0] input setup time	$T_{DI.SU}$	8			ns
SD/eMMC_D[3:0] output delay time	$T_{DO.DLY}$			8	ns

8.7 I2S

DA16200MOD provides an I2S interface. Once an I2S block receives audio data through the DMA, it sends audio data to the external port according to the I2S standard. To use the external DAC, output through the GPIO port is possible through the register setting according to the pin configuration (Table 35).

The I2S also provides a receive function. However, I2S transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by register setting. If the I2S signal is input from outside after the reception function is set, the audio signal can be decoded, stored in the FIFO, and read out through the DMA. The decodable reception function provides 8/16/24/32-bit modes and can receive either mono or stereo.

Using the I2S clock divider register, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from outside using the GPIO pin. For accurate I2S audio sampling, I2S clock source can be input to external GPIO pins. It needs to select the GPIO pin setting as the I2S clock input and apply appropriate clock source. The available I2S clock pins are shown in Table 35.

Table 35: I2S Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA1	32	O	I2S_MCLK
GPIOA5	28	O	
GPIOA9	24	O	
GPIOA0	33	O	I2S_BCLK
GPIOA4	29	O	
GPIOA8	25	O	
GPIOA3	30	O	I2S_LRCK
GPIOA7	26	O	
GPIOA2	31	I/O	I2S_SDO
GPIOA6	27	I/O	
GPIOA3	30	I	I2S_CLK_IN
GPIOA10	23	I	

8.7.1 Block Diagram

I2S has the following features:

- Master Clock Mode only
- I2S Data pin can work in either input mode or output mode
- Clock source can be "internal 480 MHz/N" (currently using 24 MHz) or "external clock source"
- Max Sampling Rate: 48 KHz
- Mono/Stereo Mode

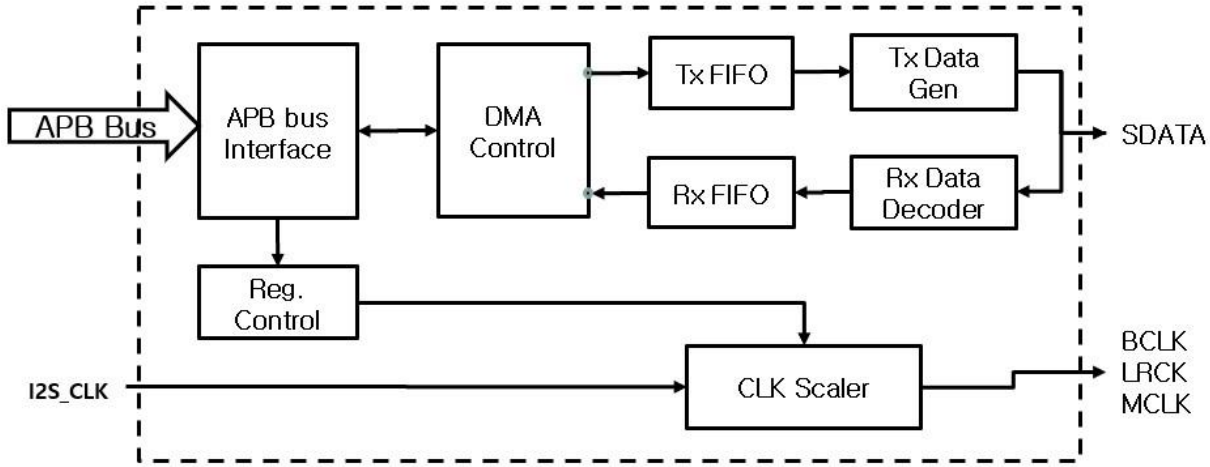

Figure 22: I2S Block Diagram

8.7.2 I2S Clock Scheme

The I2S uses a 24 MHz clock as default from the RF reference clock (40 MHz), so it can support 46.875 KHz of sampling rate. External clock sources are needed to support the standard sampling rate. See Table 36.

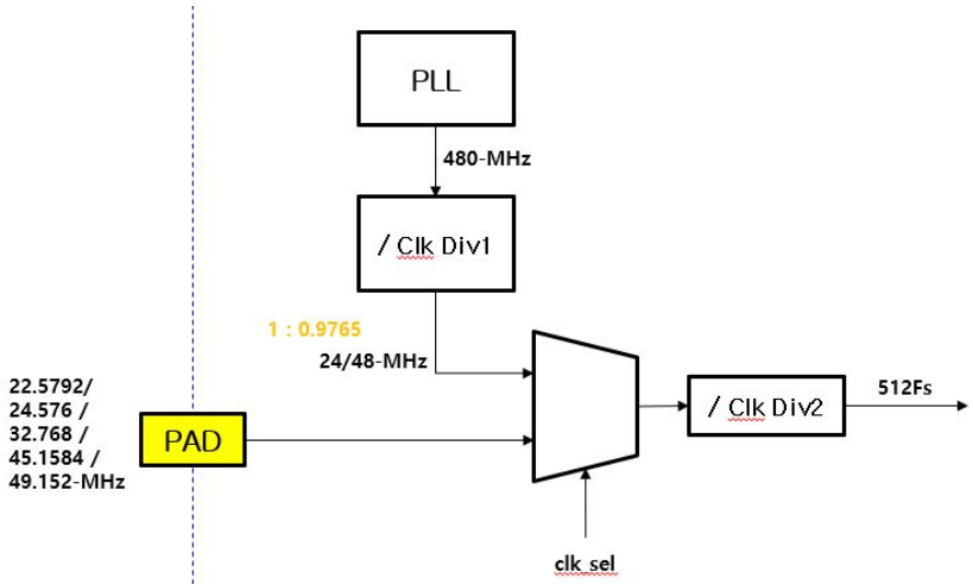

Figure 23: I2S Clock Scheme

Table 36: I2S Clock Selection Guide

Parameter										Units
LRCK	Fs	8	12	16	24	32	44.1	46.875	48	KHz
BCLK	64Fs	0.512	0.768	1.024	1.536	2.048	2.8224	3	3.072	MHz
MCLK	512Fs	4.096	6.144	8.192	12.288	16.384	22.5792	24	24.576	MHz
Clk Div2	N (=1,2,3…)	6	4	3	2	2	1	1	1	
I2S_CLK		24.576	24.576	24.576	24.576	32.768	22.5792	24 (Internal PLL)	24.576	MHz

NOTE
To confirm the exact LRCK operation, drive the Clock source at I2S_CLK.

8.7.3 I2S Transmit and Receive Timing Diagram

I2S output is possible in the following three modes. The main clock (MCLK) always outputs in 512×fs.

- I2S Mode

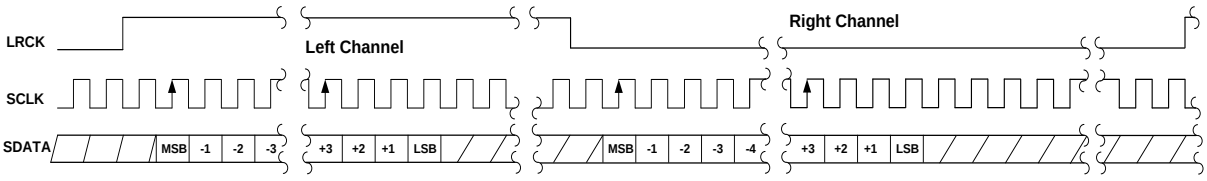

Figure 24: I2S Timing Diagram

- Left Justified Mode

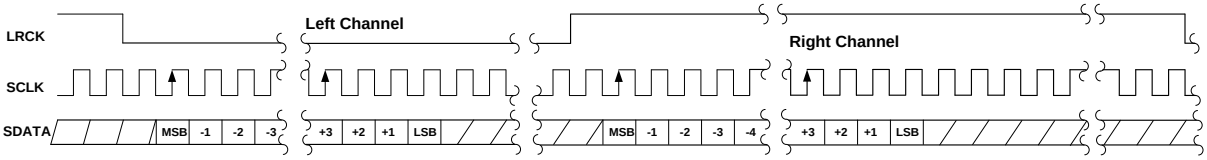

Figure 25: Left Justified Mode Timing Diagram

- Right Justified Mode

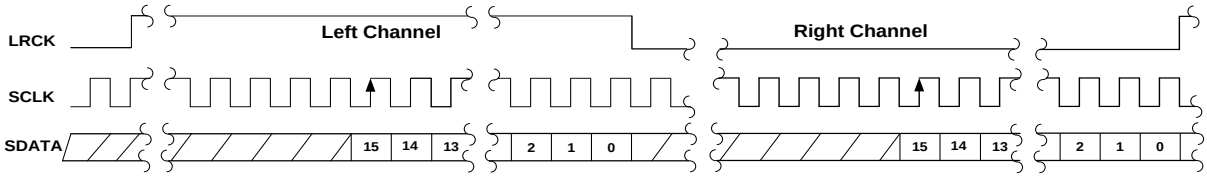

Figure 26: Right Justified Mode Timing Diagram

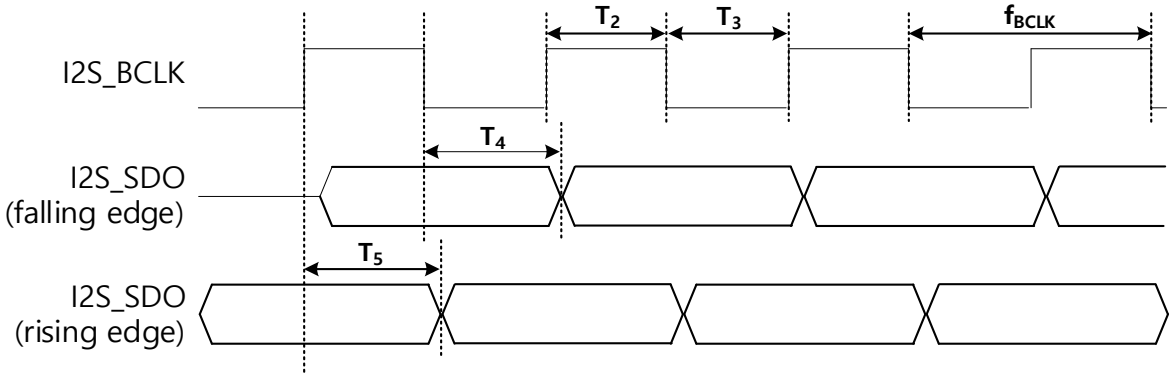

Figure 27: I2S Transmit Timing Diagram

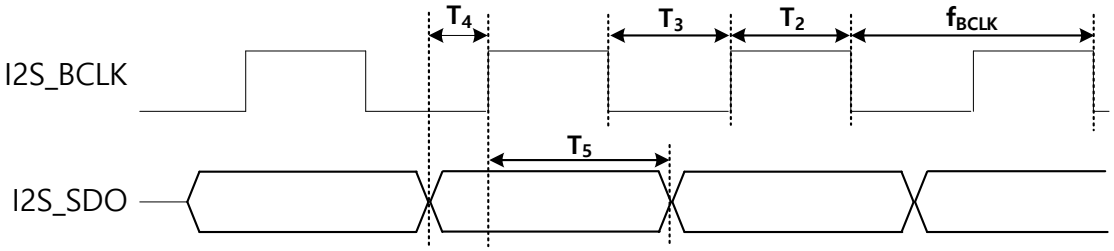

Figure 28: I2S Receive Timing Diagram

Table 37: I2S Transmit Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO output hold (falling edge)	T_4	160		-	ns
I2S_SDO output hold (rising edge)	T_5	160		-	ns

Table 38: I2S Receive Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO input setup time	T_4	15		-	ns
I2S_SDO input hold time	T_5	60		-	ns

8.8 ADC (Aux 12-bit)

8.8.1 Overview

DA16200MOD includes a high precision, ultra-low power, and wide dynamic range SAR ADC with a 12-bit resolution. It has a 4-channel single-end ADC.

Analog input is measured by four pins from GPIOA0 to GPIOA3, and pin selection is changed through the register setting.

Figure 29 shows the control block diagram.

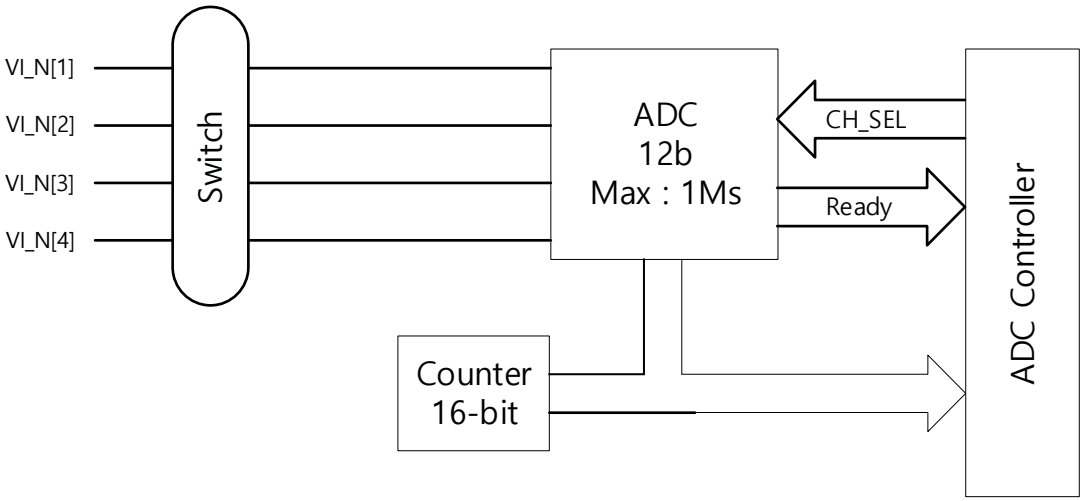

Figure 29: ADC Control Block Diagram

8.8.2 Timing Diagram

The input is digitized at a maximum of 1.0 Msps throughput rate. And the maximum input clock rate is 15 MHz.

Figure 30 shows the conversion timing, and Table 39 describes DC specifications.

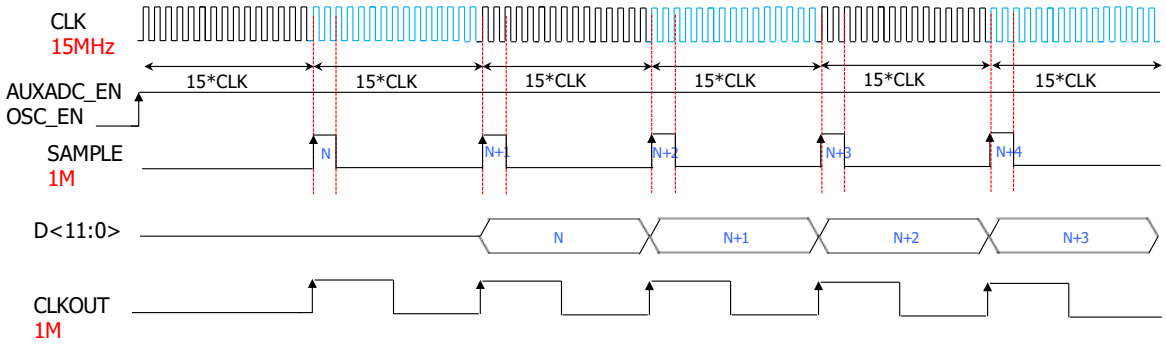

Figure 30: 12-bit ADC Timing Diagram

Table 39: DC Specification

Description	Min	Typ	Max	Unit
Resolution	4	12	12	Bits
Max clock input			15	MHz
Conversion frequency			1	MHz
Accuracy:				
• SNR • SNDR		• 61.7 • 67.2		• dB • dB
Analog input range	0		1.4	V

8.8.3 DMA Transfer

There are four ADC channel settings available. Once the input data of each channel reaches the FIFO level, it is possible to read the data through the DMA path.

8.8.4 Sensor Wake-up

DA16200MOD provides an external sensor wake-up function using the analog input signal through this Aux ADC. Even in Sleep modes, it detects the change of external analog signal, wakes up from a Sleep mode, and converts DA16200MOD into a normal operation. This function can be used in up to four channels. Also, when multiple external sensors are used, it detects analog signals while changing the channel automatically. For example, if it sets all four channels as input sources which have their threshold register respectively, in measures the channels sequentially from 0 to 3.

If one of the four values exceed the allowed range of values set by the threshold register, DA16200MOD is awaken from Sleep modes. The setting value of input change can be of two types, over threshold and under threshold.

8.8.5 ADC Ports

Table 40 shows the pin definition of the ADC.

Table 40: ADC Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOA3	30	A	Analog signal
GPIOA2	31	A	Analog signal
GPIOA1	32	A	Analog signal
GPIOA0	33	A	Analog signal

8.9 GPIO

All digital pads can be used as GPIO, and each GPIO port is mixed with a multi-functional interface. The GPIO features of DA16200MOD are listed below:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- Maskable interrupt generation based on input value change
- Possible to be output signal of PWM[3:0], external interrupt, QSPI_CSB[3:1], RF_SW[1:0], and UART_TXDOE[2:0] on the GPIO pins:
    - It provides special functions for GPIO pin use. PWM [3:0], external interrupt, QSPI_CSB [3:1], RF_SW [1:0], and UART_TXDOE [2:0] signals can be output by selecting unused pins among the GPIO pins. It is possible to select the function to be output from the GPIO register setting and select the remaining GPIO pin without using it to output the specific function to the desired GPIO pins

8.9.1 Antenna Switching Diversity

DA16200MOD-AAE4WA32 (u.FL connector type module) provides the antenna switching diversity function for performance improvement in multi-path environment. Phy block measures the RSSI of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. To use this function, an external switching element is required, and switching control is performed through the GPIO. Two GPIOs can be used for switching control, and any unused pins among the GPIO pins can be selected for this purpose. The control signal can be changed by register setting to suit the external switching device.

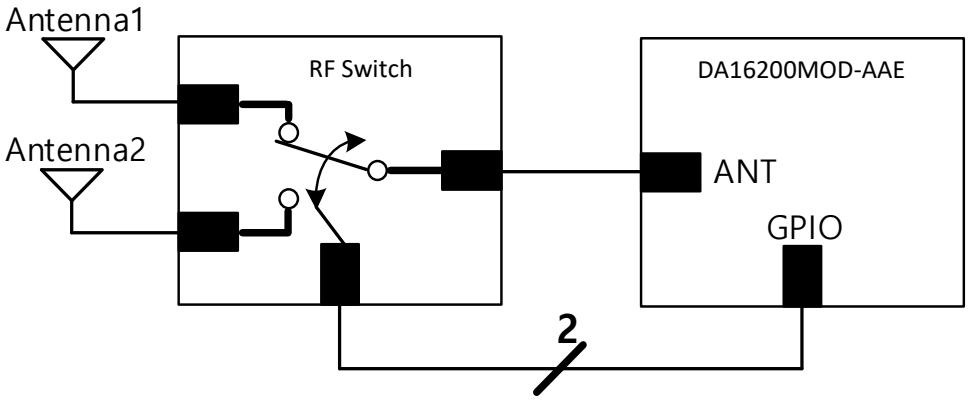

Figure 31: Antenna Switching Internal Block Diagram

If the Antenna Switching Diversity function is enabled, the function is automatically done by PHY hardware block. The basic operation scheme is as follows:

- Antenna's RSSI decision is made for 11b PPDU, except for 11g/n PPDU
- When PHY hardware detects the existence of 11b PPDU, it stores RSSI
- After it switch to another antenna, the RSSI stored and decision is made which antenna has better RSSI
- This operation is done during 11b PPDU's preamble duration to protect corruption of 11b PPDU data reception
- The decided antenna is not changed until there is a new 11b PPDU

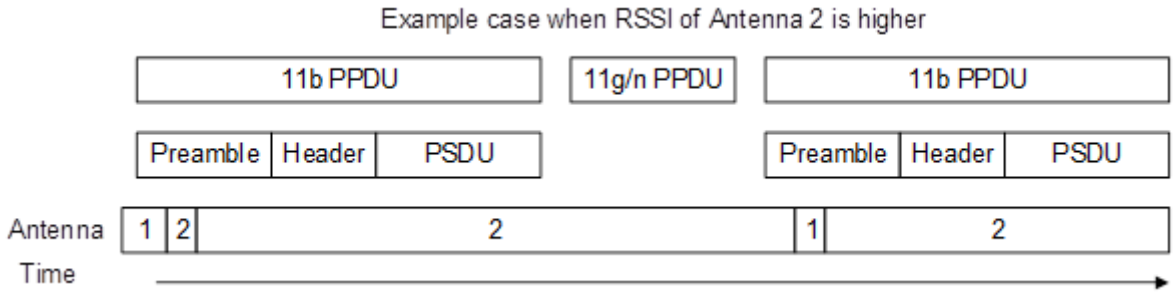

Figure 32: Antenna Switching Timing Diagram

For reference, this antenna switching diversity is different from MRC. (Maximum Ratio Combining)

8.10 UART

DA16200MOD provides 3 UARTs, features of which are described below:

- Programmable use of UART (UART1 and UART2)
- Compliance to the *AMBA AHB bus specification* [6] for easy integration into SoC implementation
- Supports both byte and word access for reduction of bus burden
- Supports both RS-232 and RS-485
- Separate 32×8 bit transmit and 32×12 bit receive FIFO memory buffers to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop and parity), which are added prior to transmission and removed on reception
- Independent masking of transmit FIFO, receive FIFO, and receive timeout
- Supports for DMA
- False start bit detection
- Programmable flow control (CTS/RTS, UART1)
- Fully programmable serial interface characteristics:
  - Data can be of 5,6,7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1- or 2- stop bit generation
  - Baud rate generation

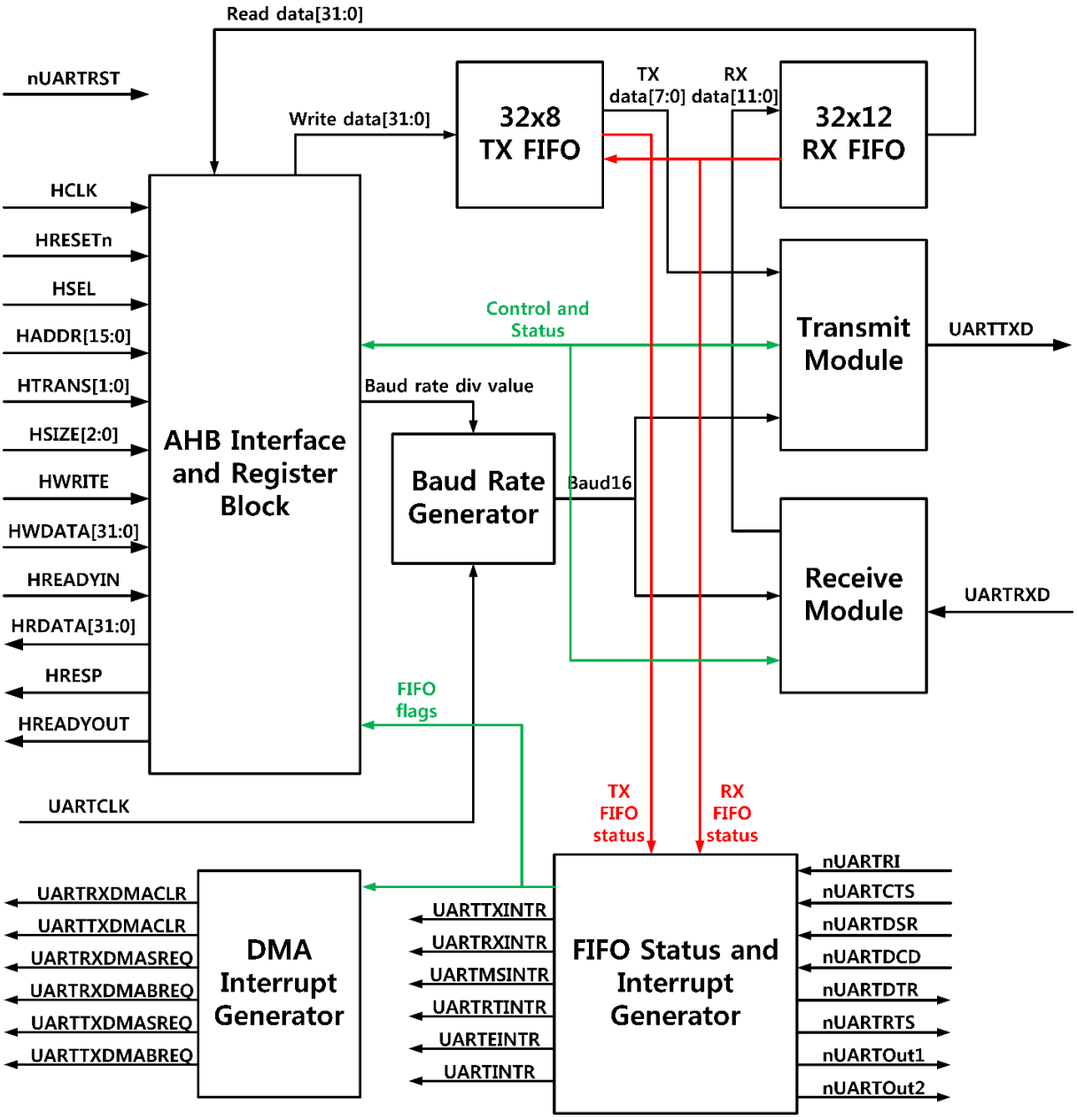

Figure 33: DA16200 UART Block Diagram

8.10.1 RS-232

As the serial communication between the UART and the selected device is asynchronous, additional bits (start and stop) are inserted to the data line to indicate the beginning and end. By these bits, two devices can be synchronized. This structure of serial data accompanied by start and stop bits is referred to as a character, as shown in Figure 34.

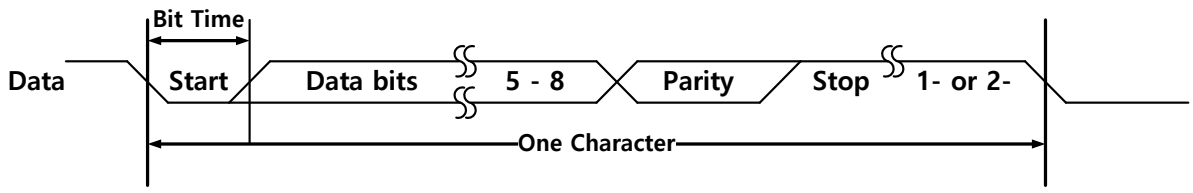

Figure 34: Serial Data Format

An additional parity bit may be added to the serial character. This bit appears between the last data bit and the stop bit(s) in the character structure. It provides the UART with the ability to perform simple error checking on the received data.

The UART Line Control Register is used to control the serial character characteristics. The individual bits of the data word are sent after the start bit, starting with the least significant bit (LSB). These are followed by the optional parity bit, followed by the stop bit(s), which can be 1 or 2.

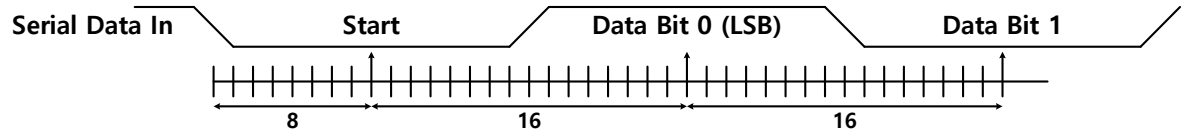

Figure 35: Receiver Serial Data Sampling Points

All the bits in the transmission are transmitted for exactly the same time duration. This is referred to as a Bit Period or Bit Time. One Bit Time equals 16 baud clocks. To ensure stability on the line, the receiver samples the serial input data at approximately the mid-point of the Bit Time, once the start bit has been detected. As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit. Figure 35 shows the sampling points of the first couple of bits in a serial character.

8.10.2 RS-485

DA16200MOD UART supports RS-485. UART485EN register (0x054) is required to be assigned to one to enable the RS-485. In order to use RS-485, additional signal (UARTTXDOE) is required to notice TXD intervals. This signal can be an output by selecting any unused pins among the GPIO pins.

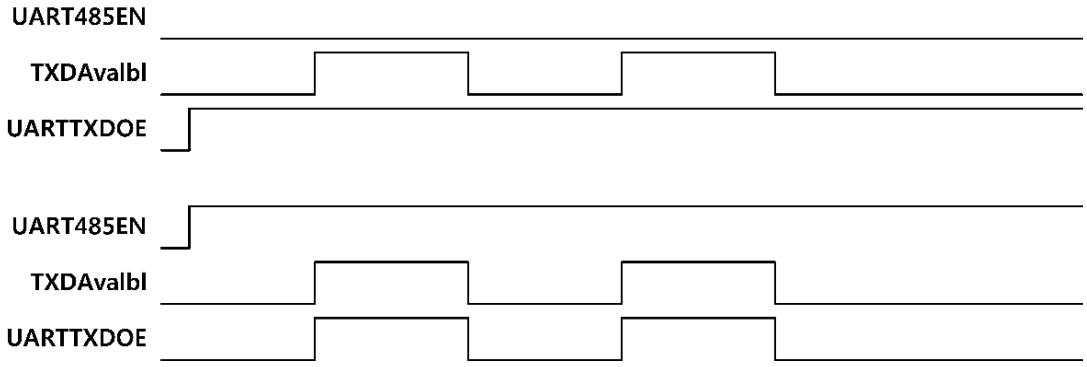

Figure 36: UARTTXDOE Output Signal for UART RS-485

8.10.3 Baud Rate

UART clock frequency (FUARTCLK) is fixed to 80 MHz. Baud Rate Divisor can be calculated as (FUARTCLK / (16 x Baud Rate)). Baud Rate Divisor is comprised of the integer part (UART_INTBRDIV) and fractional part (UART_FRABRDIV). The maximum baud rate of DA16200 UART is 2.5 MBaud.

The following example shows how to calculate the divisor value.

Example:

If the required baud rate is 921600 with 80 MHz FUARTCLK, the Baud Rate Divisor becomes

(8 x 107) / (16 x 921600) = 5.425.

This means the integer value is 5 and the fractional value is 0.425.

Then, the fraction part becomes integer ((0.425 x 64) + 0.5) = 27.

Then, generated baud rate divider is 5 + 27/64 = 5.422.

Finally, generated baud rate becomes (8 x 107) / (16 x 5.422) = 922169.

And the error between required baud rate and generated baud rate is

(922169 – 921600) / 921600 x100 = 0.062%.

8.10.4 Hardware Flow Control

Hardware flow control feature is fully selectable, and serial data flow is controlled by using nUARTRTS output and nUARTCTS input signals. Figure 37 shows how two different UART can communicate using hardware flow control.

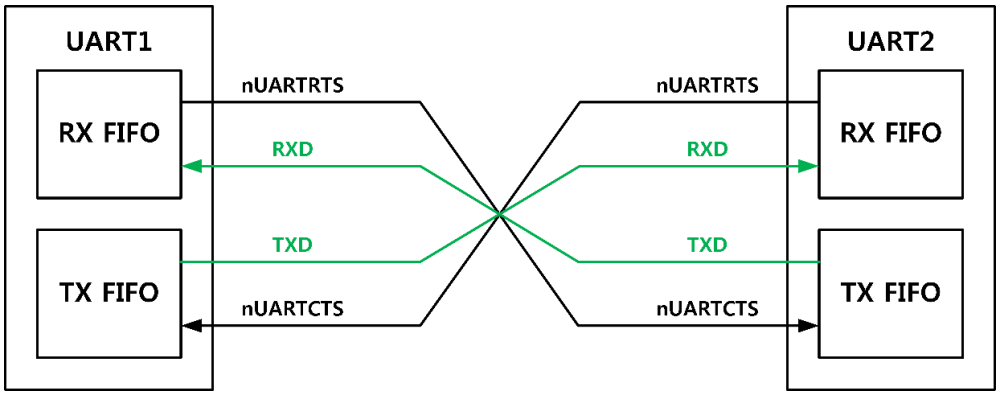

Figure 37: UART Hardware Flow Control

When RTS flow control is enabled, nUARTRTS signal is asserted until the receive FIFO is filled up to programmed level. When CTS flow control is enabled, transmitter can transmit the data when nUARTCTS signal is asserted. CTSEn (CTS enable) and RTSEn (RTS enable) bits are determined by 14th (RTS) and 15th bit (CTS) of UARTCR register.

Table 41: Control bits to enable and disable hardware flow control

CTSEn	RTSEn	Description
1	1	Both RTS and CTS flow control are enabled
1	0	Only CTS flow control is enabled
0	1	Only RTS flow control is enabled
0	0	Both RTS and CTS flow control are disabled

8.10.5 Interrupts

DA16200MOD UART block provides five interrupt signals by separate interrupt lines. Each interrupt conditions are Modem Status, Receive FIFO Request, Transmit FIFO Request, Receive Timeout and Reception Error. These conditions are logically OR'ed to provide a single combined interrupt, UARTINTR. Table 42 shows the interrupt signals.

Table 42: UART Interrupt Signals

Signal Name	Description
UARTMSINTR	UART Modem Status Interrupt
UARTRXINTR	UART Receive FIFO Interrupt
UARTTXINTR	UART Transmit FIFO Interrupt
UARTRTINTR	UART Receive Timeout Interrupt
UARTEINTR	UART Error Interrupt
UARTINTR	UART Interrupt. Five Interrupt signals are combined by OR function

8.10.6 DMA Interface

DA16200MOD UART block can generate DMA request signals with register settings by using DMA interrupt generator module to connect to DA16200 DMA Controller (DMA1). DMA operation of the UART is controlled using DMA Control Register.

DA16200MOD UART provides four DMA signals and receives two DMA signals, two signals to transmit (TXDMASREQ, TXDMABREQ) which are cleared by TX clear signal (TXDMACLR) and two signals to receive (RXDMASREQ, RXDMABREQ), which are cleared by RX clear signal (RXDMACLR).

When the DMA interface is not used, the TXDMACLR and RXDMACLR lines should be connected to a logic ‘0’.

Table 43 shows the pin definition of the UART interface.

Table 43: UART Pin Configuration

Pin Name	Pin Number	I/O	Function Name
UART0_RXD	13	I	UART0_RXD
UART0_TXD	12	O	UART0_TXD
GPIOA7	26	I	UART1_RXD
GPIOA5	28	I	
GPIOA3	30	I	
GPIOA1	32	I	
GPIOA6	27	O	UART1_TXD
GPIOA4	29	O	
GPIOA2	31	O	
GPIOA0	33	O	
GPIOA5	28	I	UART1_CTS
GPIOA4	29	O	UART1_RTS
GPIOA11	22	I	UART2_RXD
GPIOC7	10	I	
GPIOA10	23	O	UART2_TXD
GPIOC6	11	O	

8.11 PWM

Pulse Width Modulation (PWM) is a modulation technique used to encode a message into a pulse signal. The blocks are designed to adjust output pulse duration by the CPU bus clock (HCLK).

Figure 38 shows the structure of the PWM block.

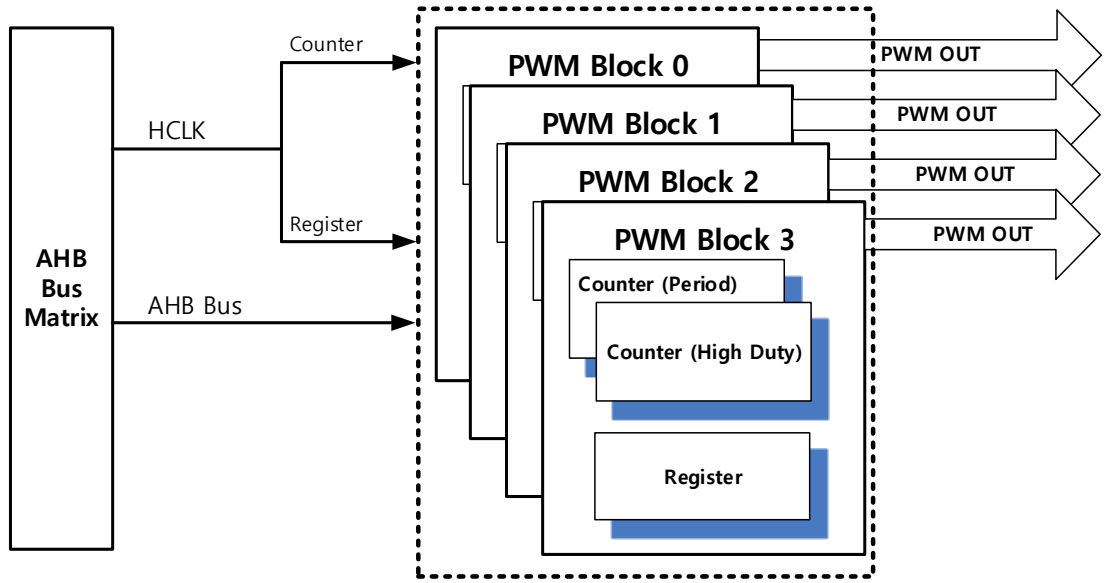

Figure 38: PWM Block Diagram

Table 44 shows the pin definition of the PWM interface. GPIOx means that PWM signals can go out through any GPIO pins via register setting.

Table 44: PWM Pin Configuration

Pin Name	Pin Number	I/O	Function Name
GPIOx			PWM[3:0] output

8.11.1 Timing Diagram

Table 45 shows the relation between the internal bus clock and PWM output wave patterns. Figure 39 show the conversion timing diagram. '**a**' and '**b**' can be adjusted through the register setting, and PWM wave patterns vary depending on the ratio. '**a**' controls the high width of pulses (nCycle High), while '**b**' controls the general cycle (nCycle Period).

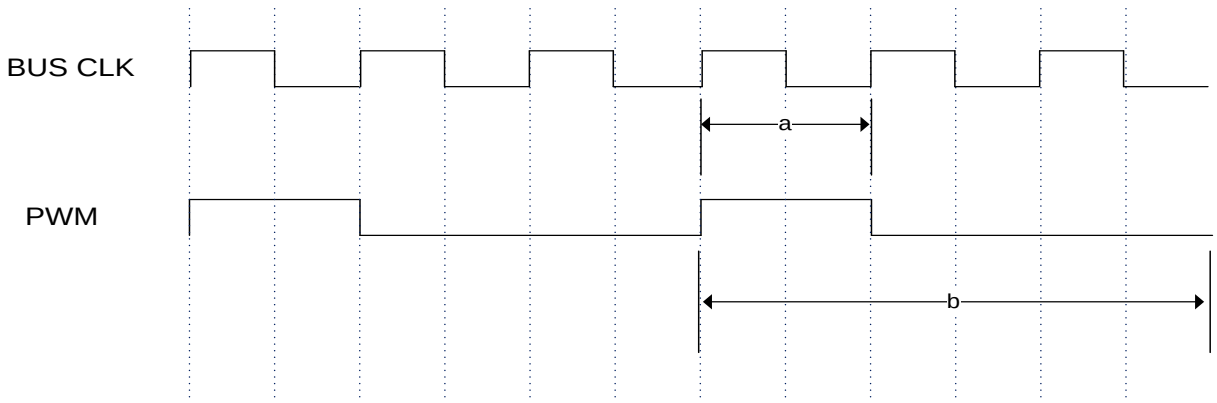

Figure 39: PWM Timing Diagram

Table 45: PWM Timing Diagram Description

Time	Description
a	Bus Clock Period × (nCycle High + 1)
b	Bus Clock Period × (nCycle Period + 1)

8.12 Debug Interface

DA16200MOD supports both IEEE Standard 1149.1 JTAG (5-wire) and the low-pin-count ARM SWD (2-wire, TCLK/TMS) debug interfaces. The SWD protocol can handle the same debug features as the JTAG.

The JTAG port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see [4].

Figure 40 shows the JTAG timing diagram.

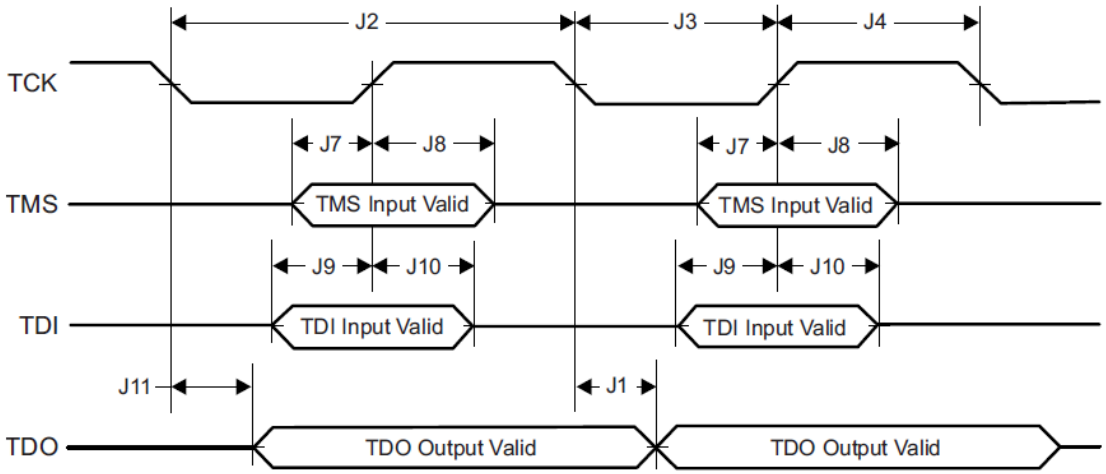

Figure 40: JTAG Timing Diagram

Table 46 shows the JTAG timing parameters.

Table 46: JTAG Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	f_{TCK}	Clock Frequency		15	MHz
J2	t_{TCK}	Clock Period		$1/f_{TCK}$	ns
J3	t_{CL}	Clock Low Period		$t_{TCK}/2$	ns
J4	t_{CH}	Clock High Period		$t_{TCK}/2$	ns
J7	t_{TMS_SU}	TMS Setup Time	1		
J8	t_{TMS_HO}	TMS Hold Time	16		
J9	t_{TDI_SU}	TDI Setup Time	1		
J10	t_{TDI_HO}	TDI Hold Time	16		
J11	t_{TDO_HO}	TDO Hold Time		15	

Table 47 shows the pin definition of the JTAG interface.

Table 47: JTAG Pin Configuration

Pin Name	Pin Number	I/O	Function Name
TMS	7	I/O	Data
TCLK	8	I	Clock
GPIOC8	9	I	TDI: Data Input
GPIOC7	10	O	TDO: Data Output
GPIOC6	11	I	nTRST: Reset

8.13 Bluetooth Coexistence

DA16200MOD provides the Bluetooth coexistence function to be properly aligned with external devices activated at 2.4 GHz.

8.13.1 Interface Configuration

The following three pins can be set in pin multiplexing:

- BT_sig0 (oWlanAct)
  - It indicates that Output, WLAN is currently active
- BT_sig1 (iBtAct)
  - It indicates that Input, BT/BLE is currently active
- BT_sig2 (iBTPri)
  - It indicates that Input (Optional), BT/BLE has a higher priority

A variety of configurable settings are available, including active high/low, manual force mode, use status of the optional iBTPri function, and whether or not to switch oWlanAct to Active in the event of TX/RX/TRX.

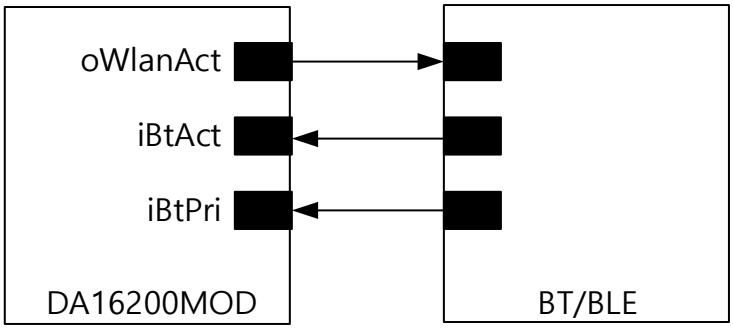

Figure 41: Bluetooth Coexistence Interface

8.13.2 Operation Scenario

The Bluetooth coexistence can be switched on/off by the configurable register, and the activation scenarios based on the status of each pin are described below:

- BT_sig0 (oWlanAct)
  - When asserted, external BT/BLE is expected to stop occupying RF
- BT_sig1 (iBtAct)
  - When asserted, DA16200MOD stops occupying RF
- BT_sig2 (iBTPri)
  - It is optional and thus may not be used

- If it is used and DA16200's iBtAct = Active while iBTPri = Non-Active, DA16200 may ignore iBtAct

9 Applications Schematic

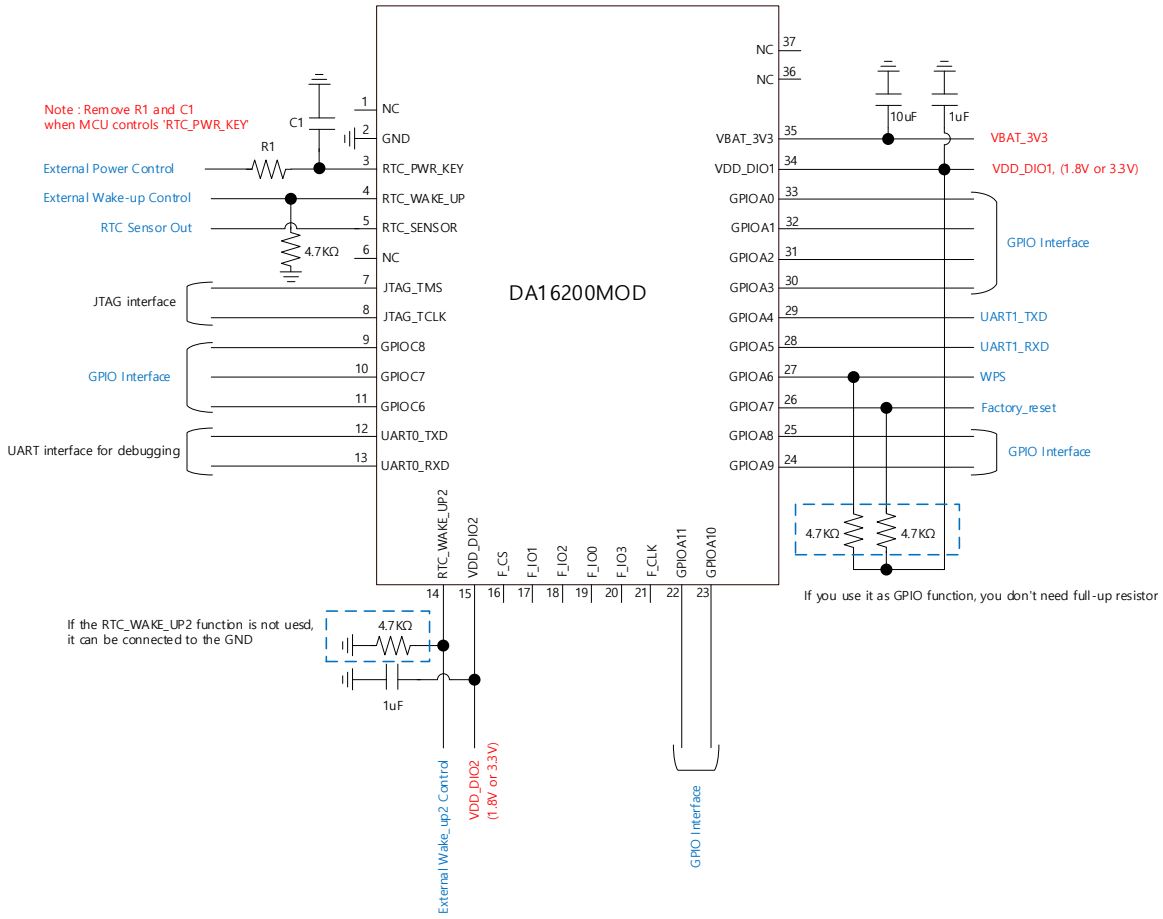

Figure 42: Application Schematic

Table 48: Component for RTC POWER KEY

Quantity	Part Reference	Value	Description
1	R1	470 kΩ	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. For detail information, See 6.1
1	C1	1uF	Remove when MCU control 'RTC_PWR_KEY'. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1uF. For detail information, See 6.1

10 Package Information

10.1 Dimension: DA16200MOD-AAC

Unit: mm

Tolerance: 13.8(±0.2) x 22.1(±0.2) x 3.3(±0.1)

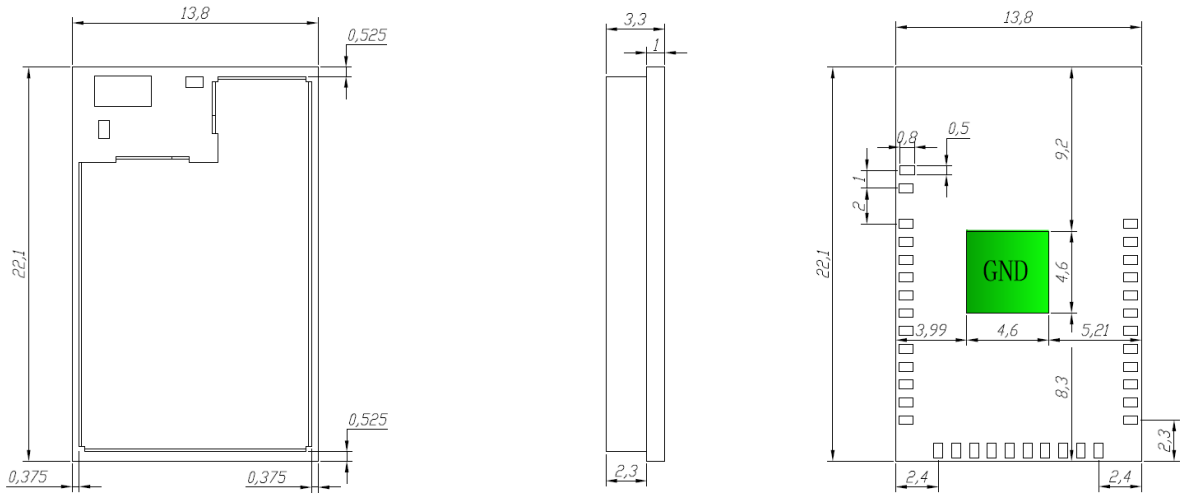

Figure 43: AAC Module Dimension

10.2 Dimension: DA16200MOD-AAE

Unit: mm

Tolerance: 13.8(±0.2) x 22.1(±0.2) x 3.3(±0.1)

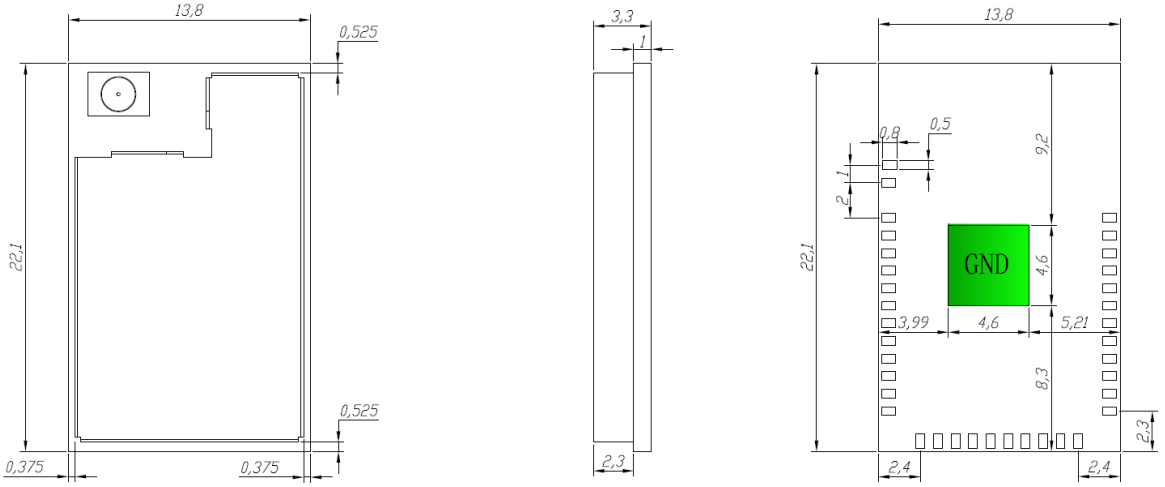

Figure 44: AAE Module Dimension

10.3 PCB Land Pattern

Unit: mm

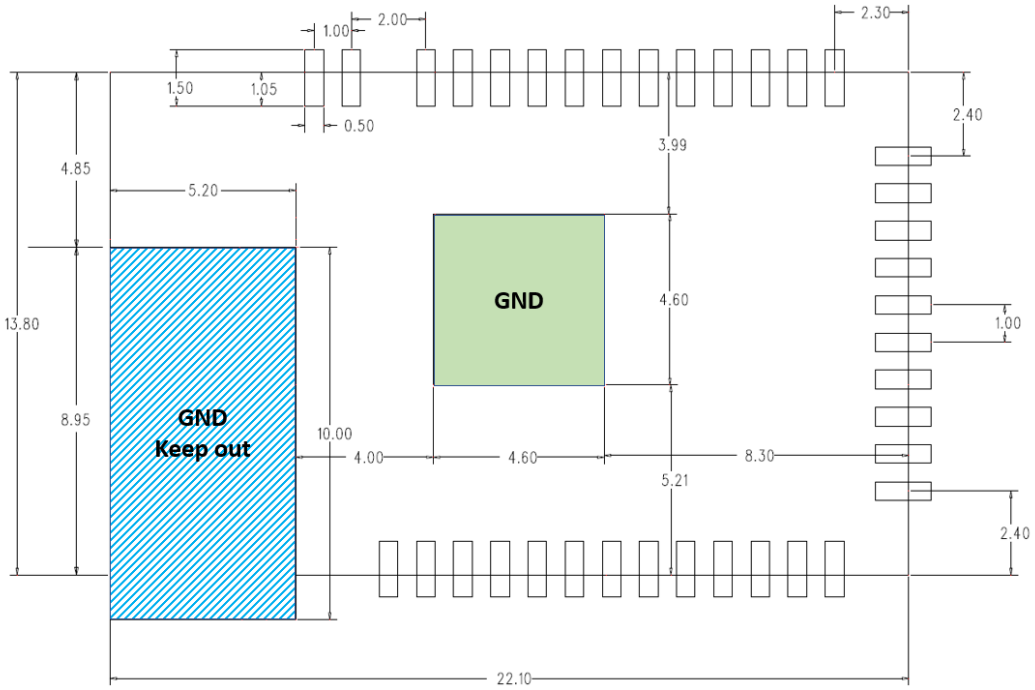

Figure 45: PCB Land Pattern (Top View)

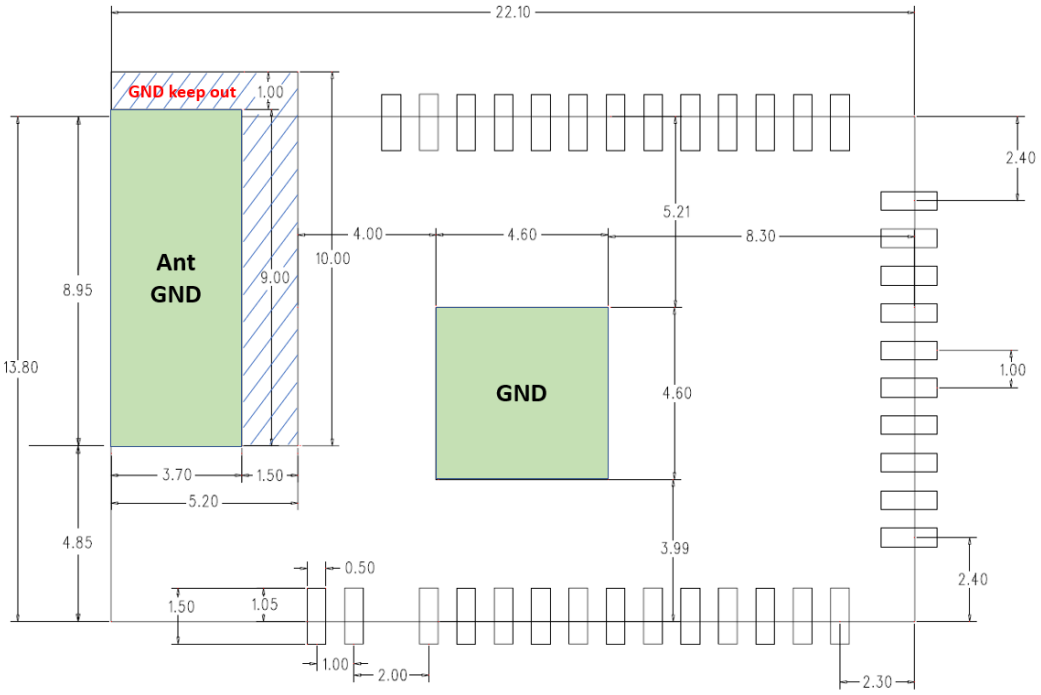

Figure 46: PCB Land Pattern (Bottom View)

Ant GND is only needed on the bottom of the PCB. GND must be removed for all layers including the inner layer except the bottom. See Figure 47 for detail.

10.4 4-Layer PCB Example

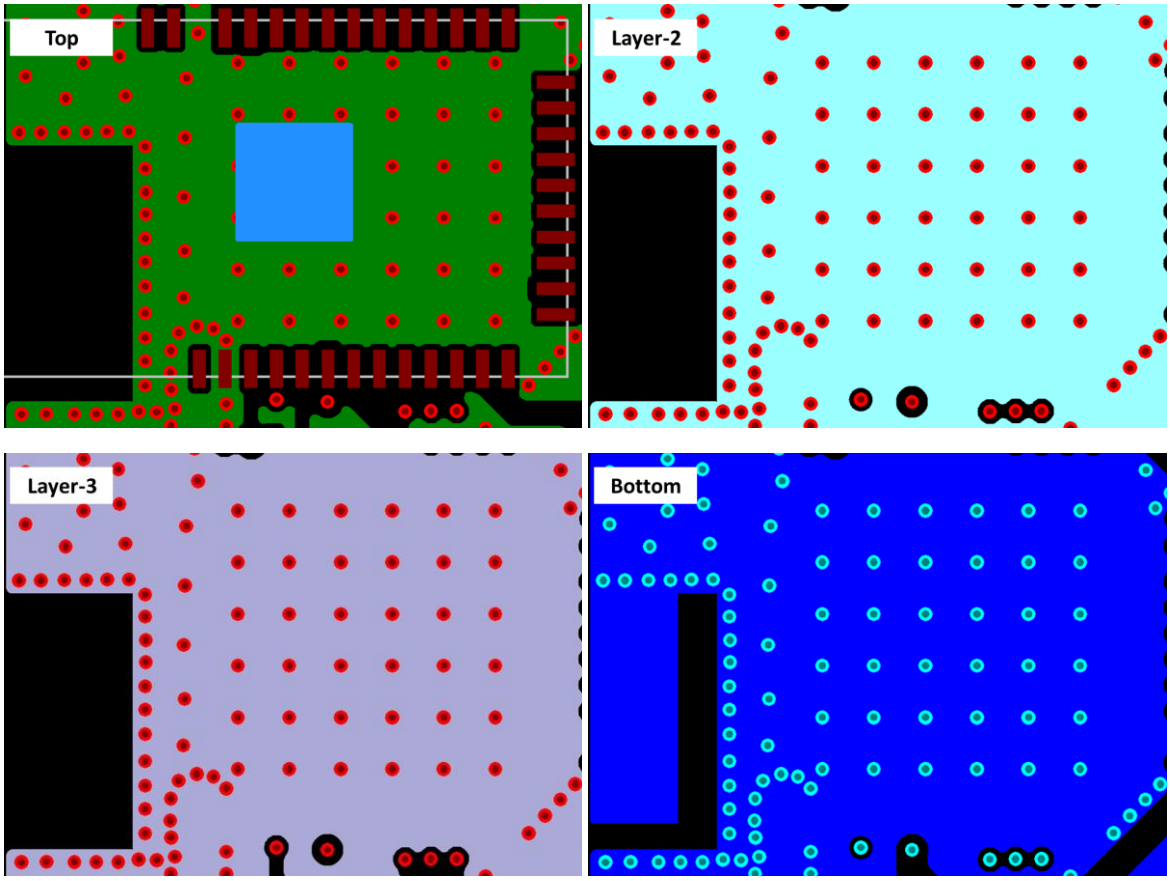

Figure 47: 4-Layer PCB Example

10.5 Soldering Information

10.5.1 Condition for Reflow Soldering

Figure 48 shows the typical process flow for mounting surface mount packages to PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacture should be followed to determine the proper reflow profile. Figure 49 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 20 to 40 seconds.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement
5. Component attachment

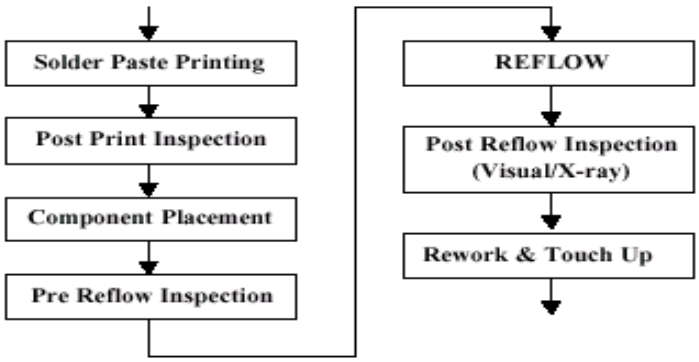

Figure 48: Typical PCB Mounting Process Flow

Table 49: Typical Reflow Profile (Lead Free): J-STD-020C

Profile Feature	Lead Free SMD
Average ramp up rate (Ts_{max} to T_p)	3 °C/s Max.
Preheat	
• Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{max} to Ts_{min})	• 150 °C • 200 °C • 60 to 180 seconds
Time maintained above	
• Temperature (T_L) • Time (t_L)	• 217 °C • 60 to 150 seconds
Peak/Classification temperature (T_p)	260 °C
Time within 5 °C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6 °C/s Max.
Time from 25 °C to peak temperature	8 minutes Max.

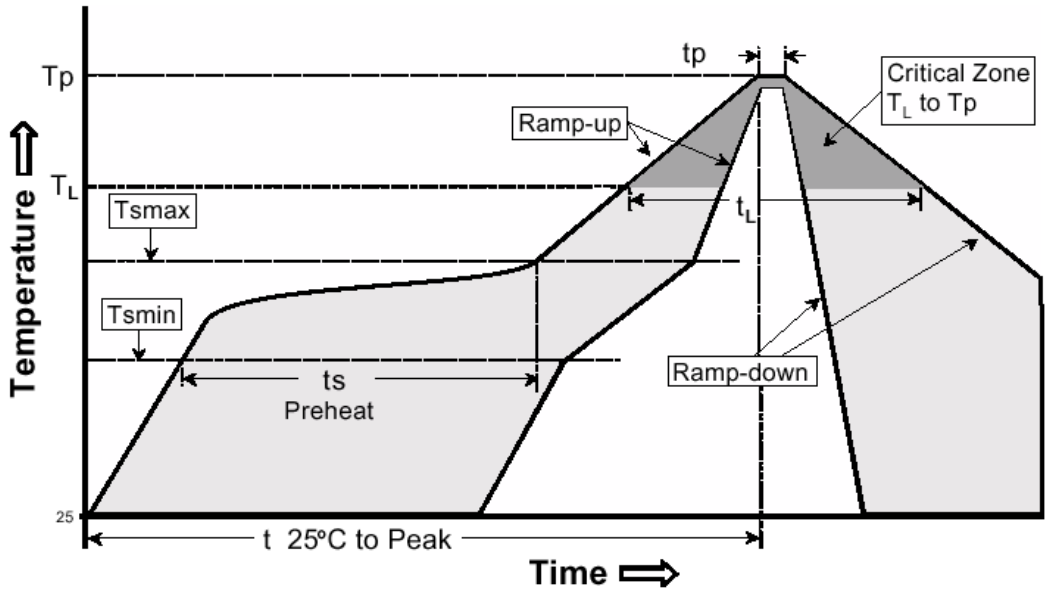

Figure 49: Reflow Condition

11 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's Website or your local sales representative.

Table 50: Ordering Information (Production)

Part Number	Pins	Size (mm)	Shipment Form	Pack Quantity
DA16200MOD-AAC4WA32	37	13.8 x 22.1 x 3.3	Reel	MOQ: 500 pcs
DA16200MOD-AAE4WA32	37	13.8 x 22.1 x 3.3	Reel	MOQ: 500 pcs

Part Number Legend:

DA16200MOD-AAC4WA32

AA: Module revision number

C: Select module type

[C] Chip antenna, [E] u.FL connector

4: Flash memory

[4] 4Mbyte, [2] 2Mbyte

W: Voltage range

[W] 3.3 V, [L] 1.8 V

A3: Package No.

2: T&R packing

Revision History

Revision	Date	Description
3.1	03-Fab-21	• Editorial • Removed BOR part • Added Note for Power on Sequence in the Section 6.1, Updated Figure 7 and Table 16 • Section 8.7.3 Fixed typo • Added Section 8.7.1 and 8.7.2 • Updated Applications Schematic

3.0	23-Jul-20	• Sync with SoC datasheet v3.1
		• Modified Chapter 3 description to Network subsystem layer.
		• Modified DA16200MOD pin Mux (Table 2)
		  ○ Added module default pin conditions
		  ○ I2C CLK GPIOA2 -> GPIOA3
		• Added chapter 5.3.3, 5.3.4
		• Modified Rx max input level in chapter 5.4.1(Table 11)
		• Updated Chapter Note 1 Sleep mode description
		• Updated RTC_PWR_KEY description and remove one sentence which leads to misunderstanding. Table 17
		• Modified I2C timing in table Table 30, Table 32
		• Added description of chapter 8.9.1
		• Updated Chapter 9 application schematics
		• Changed Module dimension picture **Error! Reference source not found.**, **Error! Reference source not found.**
		• Removed F_xx pins
		• Changed the link from customer support portal to Dialog website
		• Added PCB land pattern Figure 46, Figure 47

2.0	08-May-20	• Added Tolerance of dimension • Added min/max Radio characteristics in Table 11, Table 12and Table 13 • Modified Chapter 8.10.3 Baud rate • Updated Reach and ROHS compliance
0.4	07-Apr-20	• Updated Key Features • Modified DA16200MOD pin Mux Table 2 • Chapter 7.4 Pulse Counter added • Chapter 8.10.1 RS-232 added
0.3	23-Mar-20	• Added ESD performance, Table 15 • AC characteristics and current consumption of data updated in Table 11, Table 12 and Table 13 • Updated Key Features, about clock source & embedded memory
0.2	22-Oct-19	• Modified module size
0.1	03-Oct-19	• Preliminary datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

Reach and RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of REACH and Directive 2015/863/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request. Module does not have to be HF.

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