Datasheet

APM32F103xDxE

Arm® Cortex®-M3 based 32-bit MCU

Version: V 1.6

1 Features

System Architecture

- 32-bit Arm® Cortex®-M3 core
- 96MHz Maximum Frequency

Clock and memory

- HSECLK: supports 4~ 16MHz external crystal oscillator
- LSECLK: supports 32.768KHz RTC oscillator
- HSICLK: factory calibrated 8 MHz RC oscillator
- LSICLK: 40 KHz RC oscillator
- Flash up to 512 KB
- SRAM up to 128 KB
- EMMC: Supports CF card, SRAM, PSRAM, SDRAM, NOR and NAND memory
- Parallel LCD interface, compatible with 8080/6800 mode

Power supply and low power

- Reset power supply voltage 2.0V~3.6V
- Support PVD
- Support sleep, stop and standby modes
- V_{BAT} power supply can support RTC and standby register work

FPU

- Independent FPU module supports floating point operations

ADC and temperature sensor

- 3x 12-bit accuracy ADCs, up to 21 input channels
- ADC voltage conversion range: 0~V_{DDA}
- Support dual sampling and hold functionTemperature sensor: 1

2x12-bit DAC

I/Os

- 112/80/51 I/Os, depend on package type
- All mappable on 16 external interrupt vectors

12-channel DMA controller

- 2 DMAs, up to 7 independent configurable channels

Timer

- 2x16-bit advanced timers TMR1/8 with support for dead-zone control and emergency braking
- 4x16-bit universal timer TMR2/3/4/5, each timer has 4 independent channels to support input capture, output comparison, PWM and pulse counting functions
- 2x 16-bit basic Timers TMR6/7
- 2 watchdog Timers (Independent and Window)
- 1 SysTick Timer: a 24-bit downcounter

Communication Interfaces

- 3xUSART, 2xUART, support ISO 7816,LIN and IrDA
- 2 x I2C support SMBus/PMBus
- 3 x SPI (2 reusable non-I2s), maximum transmission speed is 18Mbps
- 1x USBD
- 1xCAN 2.0B support USBD and CAN work independently at the same time
- 1xSDIO

1xCRC Unit

support 96 - bit not rewrite the only ID

SWD and JTAG debug interface

Package

- LQFP64/100/144

Application

- Medical equipment, PC peripherals, industrial control, intelligent instruments and household appliances

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2 Overview

32-bit APM32F103xDxE series MCU is based on the Arm® Cortex®-M3 core. The maximum operating frequency is 96MHz.

Built-in high-speed memory (Flash up to 512Kbytes and SRAM up to 128Kbytes), a number of enhanced I/Os ports and peripherals to connect to 2 APB buses.The chip is equipped with a powerful FPU, which supports single-precision data processing instructions and data types. All models include 3 12-bit ADC, 4 universal 16-bit timers and 2 PWM timers, 2 basic timers, as well as standard and advanced communication interfaces: 2 I2C, 3 SPI, two I2S, 1 SDIO, 3 USART, 2 UART,1 USBD, and 1 CAN.

APM32F103xDxE enhanced series operates temperature rang from -40℃~ +105℃, Voltage range: 2.0V ~ 3.6V. A series of power-saving modes ensure the requirements of low power consumption applications.

APM32F103xDxE enhanced series MCU support 3 different packages from 64 ~ 144 pins. The configuration of peripherals in the device is different according to different package forms.

3 Features Description

Please refer to the table below for details of APM32F103xDxE product features and peripheral counts.

Table 1 APM32F103xDxE Product Features and Peripheral Configurations

peripheral		APM32F103Rx		APM32F103Vx		APM32F103Zx	
		RD	RE	VD	VE	ZD	ZE
Flash（Kbytes）		384	512	384	512	384	512
SRAM (Kbytes)		64	128	64	128	64	128
Memory Controller(EMMC)		No		Yes（Do not support SDRAM）		Yes(Support SDRAM)	
Timers	General-purpose	4					
	Advanced	2					
	Basic	2					
Comm	SPI（I^2S）	3（2）					
	I^2C	2					
	USART（UART)	3（2）					
	USBD	1					
	CAN	1					
	SDIO	1					
	GPIOs	51		80		112	
12-bit ADC（Number of channels）		3 16		3 16		3 21	
12-bit DAC（Number of channels）		2 2					
CPU frequency		96MHz					
FPU		1					
Operating voltage		2.0 ~ 3.6 V					
Package		LQFP64		LQFP100		LQFP144	

3.1 Arm® Cortex®-M3 Core with Embedded Flash and SRAM

Arm® Cortex®-M3 processor is the latest generation of Arm processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

Arm® Cortex®-M3 is 32-bit RISC processor provides additional code efficiency and exploits the high performance of ARM core on the storage space of the usual 8-bit and 16-bit systems.

APM32F103xDxE enhancedseries MCUs are based on ARM core, so it is compatible with all ARM tools and software.

Figure 4 Functional block diagram

3.2 Memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

Table 2 Description of Memory

Memory	The biggest byte	Function
Embedded Flash	512 Kbytes	For storing programs and data
Embedded Static Memory	128Kbytes	CPU can be accessed (read/write) with 0 wait cycle.

3.2.1 Configurable External Memory Controller

APM32F103xDxE enhanced series integrates EMMC modules, consisting of SMC, DMC and supports PC /CF card, SRAM, SDRAM, PSRAM, NOR and NAND.

Function is introduced:

- Three EMMC interrupt source, through logic or even to the NVIC unit
- Write FIFO
- Code outside the NAND flash memory and the PC card file operation

3.3 Power Management

3.3.1 Power Supply Schemes

Table 3 Power Supply Schemes

Name	Voltage Range	Description
V_{DD}	2.0 ~ 3.6V	V_{DD} supplies power directly to the IO port, and in addition, the V_{DD} supplies power to the core circuit via a voltage regulator
V_{SSA}/V_{DDA}	2.0 ~ 3.6V	Power the analog portion of the ADC, DAC, reset module, RC oscillator and PLL.When using ADC or DAC, VDDA must not be less than 2.4V. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
V_{BAT}	1.8V ~ 3.6V	When V_{DD} is turned off, power is supplied to the RTC, external 32kHz oscillator, and backup registers via an internal power switcher.

Note: Refer to details on how to connect power pins in Figure 10.

3.3.2 Voltage Regulator

The voltage regulator can adjust the working mode of the MCU to reduce power consumption. There are three operation modes:

Table 4 Operation Modes of Voltage Regulator

Name	Description
Main Mode(MR)	MR is used in nominal regulation mode
Low Power Mode(LPR)	LPR is used in the stop modes
Power Down Mode	For the standby mode of CPU, the output of the voltage regulator is in the high resistance state, the power supply of the kernel circuit is cut off, the voltage regulator is in the zero consumption state, and the contents of registers and SRAM are all lost.

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

3.3.3 Power Supply Supervisor

The product is integrated with POR and PDR circuit.This circuit is always in the working state to ensure that the system works when the power supply exceeds 2V. When the V_{DD} is lower than the set threshold $V_{POR/PDR}$, the system will keep the reset state without connecting the external reset circuit.

The product monitors the V_{DD}/V_{DDA} voltage through the PVD and compares the monitored voltage to the threshold V_{PVD}. Interrupts occur when the V_{DD} is below or above the set threshold V_{PVD}. The interrupt handler can issue a warning message or switch the microcontroller to safe mode.The PVD function needs to be enabled programmatically.

Refer to Chapter 5 Electrical Characteristics for details on VPOR/PDR and V_{PVD}.

3.3.4 Low Power Mode

The product supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

Table 5 Low Power Mode

Mode Types	Description
Sleep Mode	In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
Stop Mode	The stop mode minimizes power consumption while maintaining no loss

Mode Types	Description
	of SRAM and register contents.In shutdown mode, the internal 1.5V power supply section stops, the PLL, HSICLK's RC oscillator and HSECLK crystal oscillator are turned off, and the voltage regulator is placed in either normal mode or low power mode.The microprocessor can be woken from shutdown mode by any signal configured to EINT.The EINT signal can be one of 16 external I/O ports, the output of a PVD, a wake-up call from an RTC alarm clock or a USBD.
Standby Mode	The lowest power consumption can be achieved in standby mode.In standby mode, the internal voltage regulator is turned off, so the power supply to the internal 1.6V part is cut off.PLL, HSICLK RC oscillator and HSECLK crystal oscillator are also shut down;After entering standby mode, the contents of the SRAM and registers disappear, but the contents of the backup registers remain, and the standby circuit is still working. Exiting from standby mode is when an external reset signal on the NRST, an IWDT reset, a rising edge on the WKUP pin, or an alarm clock on the RTC is available.

Note: The RTC, the IWDT, and the corresponding clock sources are not stopped by entering stop or standby mode.

3.4 Clocks and Startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary(for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 96 MHz.

Figure 5 Details on the clock tree.

3.5 RTC and Backup Registers

The RTC and the backup register are powered by a switch that selects the V_{DD} power supply if the V_{DD} is available, or the V_{BAT} pin power supply if not.Backup registers (42 16-bit registers) can be used to hold 84bytes of user application data when V_{DD} is turned off.The RTC and

backup registers are not reset by the system or power reset source, nor are they reset when awakened from standby mode.

Real-time clocks have a set of continuously running counters, can provide calendar functionality through the appropriate software, and also have alarm interrupts and phased interrupts.Its clock source can choose from an external 32.768 kHz crystal oscillator, resonator or oscillator, an internal 40 kHz low speed RC oscillator or an external high speed clock with a 128 frequency divider.To compensate for the deviation of the natural crystal, the clock of the RTC can be calibrated by output a 512Hz signal.The RTC has a 32-bit programmable counter that is used to alarm long-term measurements using the comparison register.There is a 20-bit pre-divider for the time-based clock, which by default will produce a 1-second long time reference from a 32.768kHz clock.

3.6 Boot Modes

At boot time, the bootstrap pin allows you to select one of three bootstrap modes to bootstrap from user flash memory, from system memory, or from internal SRAM.The Boot loader is stored in the system memory, and the flash memory can be reprogrammed using USART1.

3.7 CRC Calculation Unit

The CRC (Cyclic Redundancy Check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of time and stored at a given memory location.

3.8 General Purpose IO Port

51/80/112 I/Os are available for the product, and the specific selection can refer to the model and package. All I/O can be mapped to 16 external interrupt controllers, and most of I/O support 5V logic level input.

3.9 Interrupt Controller

3.9.1 Nested Vectored Interrupt Controller (NVIC)

APM32F103xDxE embeds a nested vectored interrupt controller able to handle up to 65 maskable interrupt channels(not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core

- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EINT can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

3.10 FPU

The product has built-in independent FPU floating-point operation processing unit, supports IEEE754 standard, supports single-precision floating-point operation, and supports algorithms such as CMP, SUM, SUB, PRDCT, MAC, DIV, INVRGSQT, RGSQT, SUMSQ, DOT, floating-point to integer conversion and integer to floating point conversion.

3.11 DMA

The flexible 12-channel general-purpose DMAs(7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control Timers TMRx, DAC, I^2S, SDIO and ADC.

3.12 Timer

The enhanced series of high-density APM32F103xDxE includes up to two advanced-control Timer (TMR1, TMR8), up to four general-purpose Timers, two basic Timers, two watchdog Timers, and a SysTick Timer.

Table 6 compares the features of the advanced-control, general-purpose and basic Timers:

Table 6 Timer Feature Comparison

Type of Timer	SysTick Timer	Basic Timer		General-purpose Timer				Advanced -control Timer	
Timer Name	Sys Tick Timer	TMR6	TMR7	TMR2	TMR3	TMR4	TMR5	TMR1	TMR8
Counter Resolution	24-bit	16-bit		16-bit				16-bit	
Counter Type	Down	Up		Up, down, up/down				Up, down, up/down	
Prescaler Factor		Any integer between 1 and 65536		Any integer between 1 and 65536				Any integer between 1 and 65536	
DMA Request generation		Yes		Yes				Yes	
Capture/Compare Channels		0		4				4	
Complementary Outputs		No		No				Yes	
Function Specification	– Dedicated for OS – Automatic reload function – Maskable system interrupt generation when the counter reaches 0 – Programmable clock source	– Used for DAC trigger generation – Can be used as a generic 16-bit time base		– Synchronization or event chaining function provided. – Counters can be frozen in debug mode – Can be used to generate PWM outputs – Each Timer has independent DMA request generation. – It can handle quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.				– Complementary PWM outputs with programmable inserted dead-Times – If configured as a general-purpose 16-bit Timer, it has the same features as the TMRx Timer. – If configured as the 16-bit PWM generator, it has full modulation capability (0-100%). – In debug mode, the advanced-control Timer counter can be frozen and the PWM outputs disabled. – Synchronization or event chaining provided.	

3.13 Watchdog

APM32F103xDxE series MCU has two built-in watchdogs, providing increased security, time accuracy and flexibility of use.Two watchdog devices (standalone watchdog and window watchdog) can be used to detect and resolve faults caused by software errors;When

the counter reaches a given timeout value, either triggers an interrupt (for windowed watchdog only) or produces a system reset.

Table 7 Watchdog

Watchdog	Counter Resolution	Counter Type	Prescale Factor	Function Specification
Independent Watchdog	12-bit	down	Any integer between 1 and 256	It is clocked from an independent 40 kHz internal RC oscillator and as it operates independently from the main clock, it can operate in stop and standby modes. Reset the device when a problem occurs. As a free-running Timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.
Window Watchdog	7-bit	down	-	It can be set as free-running. Reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability. The counter can be frozen in debug mode.

3.14 Peripheral Interface

3.14.1 I²C Bus

Two embedded I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes. They support 7/10-bit addressing mode and 7-bit dual addressing mode(as slave). A hardware CRC generation/verification is embedded. They can be served by DMA and they support SM Bus 2.0/PM Bus.

I²C 3/4 bus is a two-wire serial interface, composed of serial data line (SDA) and serial clock (SCL), which can work as transmitter and receiver in standard mode, fast mode and high speed mode. The fast mode and high speed mode devices are backwards compatible.

3.14.2 I²S Bus

Two standard I2S interfaces(multiplexed with SP12 and SPI3)are available,that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution,as input or output channels. Audio sampling frequencies from 8 kHz up to 48 KHz are supported. When either or both of the I2S interfaces are configured in master mode, the master clock can be output to the extemal DAC/CODEC at 256 times the sampling frequency.

3.14.3 USART

The high-capacity APM32F103xDxE enhanced series includes three universal synchronous/asynchronous transceivers (USART1, USART2 and USART3) and two universal asynchronous transceivers (UART4 and UART5).

These five interfaces provide asynchronous communication, support for IRDA SIR ENDEC transport codec, multi-processor communication mode, single-wire semi-duplex communication mode, and LIN master/slave functionality.

The USART1 interface can communicate at a rate of 4.5Mbit/s, while other interfaces can communicate at a rate of 2.25Mbit/s.

USART1, USART2 and USART3 have hardware CTS and RTS signal management, compatible with ISO7816 smart cards and SPI-like communication mode, except UART5 all other interfaces can use DMA operation.

3.14.4 SPI

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

3.14.5 Controller Area Network (CAN)

The CAN is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.14.6 USBD

The product embeds a module USBD compatible with full-speed USBD. The USBD device implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSECLK crystal oscillator).

3.14.7 Simultaneous Use of USBD and CAN Interface

When USBD and CAN are used together, you need to:

- Write 0x00000001 at the base address offset 0x100 of the USBD.
- The PA11 and PA12 pins are for USBD and CAN is used to multiplex other pins.

Note: With USBD and USBD2 common pin, so the same time CAN only use a USBD, when need to use USBD and at the same time CAN only use USBD2 instead of USBD.

3.14.8 LCD Parallel Interface(LCD)

The EMMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

3.14.9 SDIO

An SD/SDIO/MMC host interface is available,that supports MMC System Specification Version 4.2 in three different databus modes: 1-bit(default), 4-bit and 8-bit The interface allows data transfer at up to 48 MHz in 8-bit mode,and is compliant with SD Memory Card Specifications Version 2. 0.

The SDIO Card Specification Version 2. 0 also supports two different databus modes: 1-bit(default)and 4-bit.

The current version supports only one SD/SDIO/MMC4 2 card at any one time and a stack of MMC4. 1 or previous.

In addition to SD/SDIO/MMC,this interface is also fully compliant with the CE-ATA digital protocol Rev1. 1.

3.14.10 GPIO

The product can have up to 112 GPIO pins, each pin can be configured by the software for output (push pull or leak), input(with or without pull-down or pull-down) or multiplexed peripheral function ports.Most GPIO pins are shared with digital or analog multiplexing peripherals.All GPIO pins have high current flow capability.

If needed, the peripheral function of the I/O pin can be locked with a specific operation to avoid accidental writes to the I/O register.

3.15 Converters

3.15.1 ADC

Embedded in the product are three 12-bit analog/digital converters that share up to 21 external channels per ADC for single or scan conversion.In scan mode, the conversion automatically runs on a selected set of analog inputs.

other on ADC interface logic functions including synchronous sampling and maintaining, cross sampling and maintained and a single sample.The ADC can use DMA operations.

The analog watchdog function allows very precise monitoring of one, multiple, or all selected channels, with interruptions occurring when the monitored signal exceeds a preset threshold.

Events generated by the Universal Timer (TMRX) and the Advanced Control Timer (TMR1 and TMR8) can be internally cascaded to the start and injection triggers of the ADC, respectively, and applications can synchronize the AD transformation with the clock.

Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature, and the conversion range is between 2V and 3.6V.The temperature sensor is internally connected to an input channel of the ADC12_IN16 to convert the output voltage of the sensor into a numeric value.

3.15.2 Temperature Sensor

The temperature sensor generates a voltage that varies linearly with temperature. The conversion range is 2 V~3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.15.3 Digital/Analog Converter(DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration. This dual digital interface supports the following features:

·two DAC converters:one for each output channel

·8-bit or 12-bit monotonic output

·left or right data alignment in 12-bit mode

·synchronized update capability

·noise-wave generation

·triangular-wave generation

·dual DAC channel independent or simultaneous conversions

·DMA capability for each channel

·external triggers for conversion

·input voltage reference V_{REF+},

Eight DAC trigger inputs are used in the APM32F103xDxE performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.16 Debug Interface (SWJ-DP)

The Arm SWJ-DP interface is embedded, and it combines JTAG and serial wire debug that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.17 Embedded Trace Macrocell (ETM)

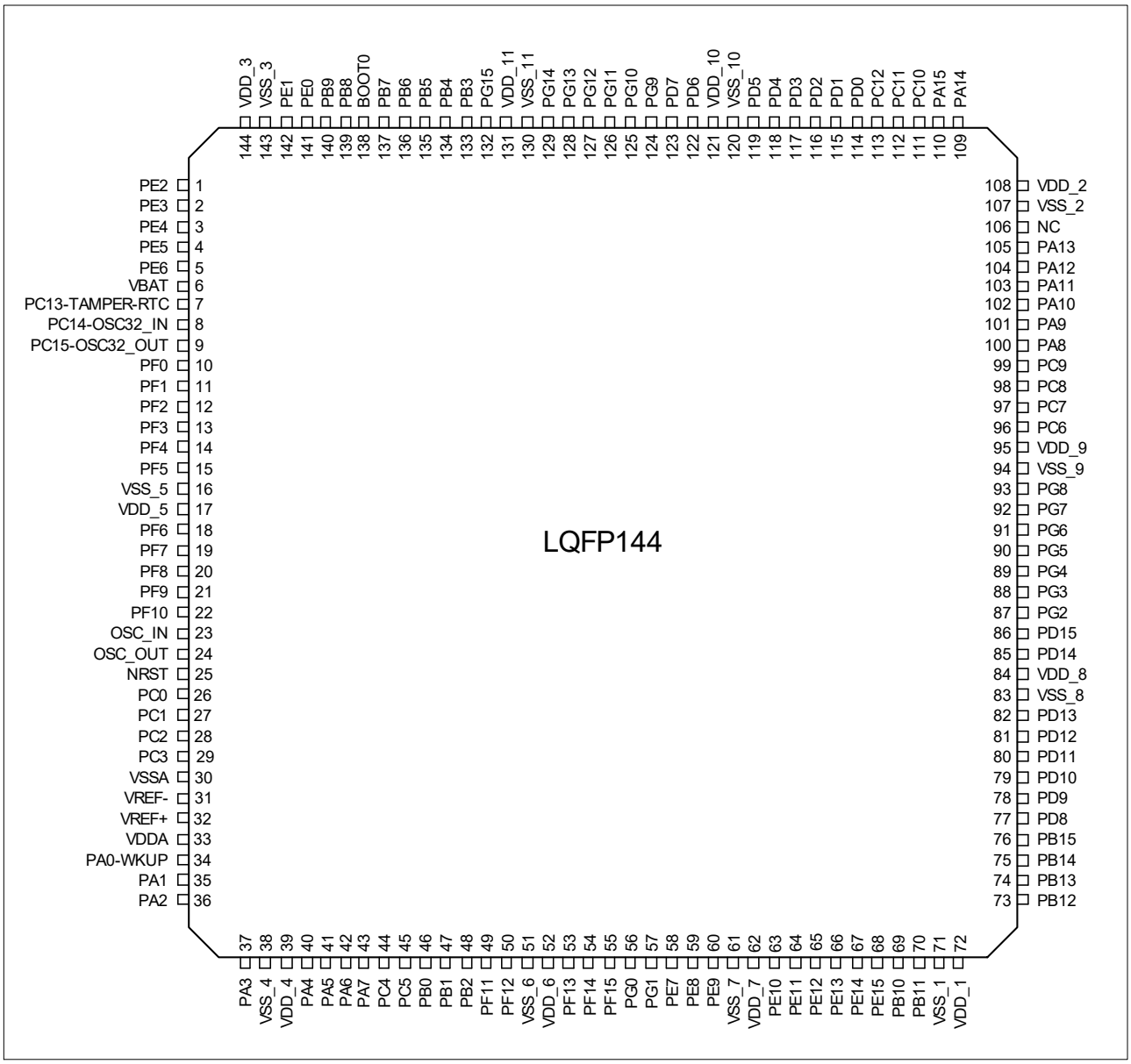
The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the APM32F103xDxE through a small number of ETM pins to an external hardware trace port analyzer(TPA)device. The TPA is connected to a host computer using USBD, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors, and is compatible with third party debugger software tools.

4 Pin Features

4.1 Pinouts and Pin Descriptions

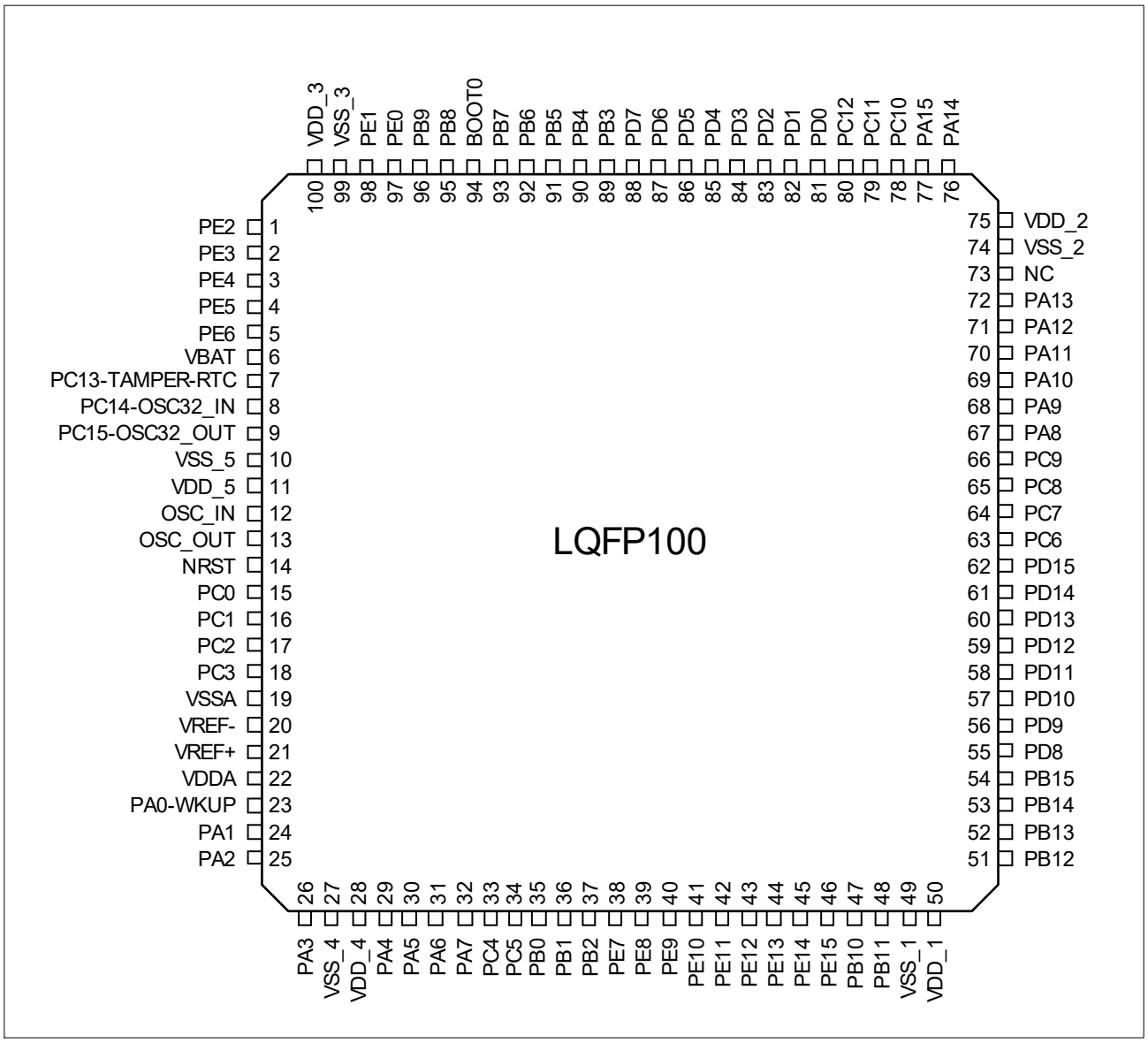
4.1.1 APM32F103xDxE Performance line LQFP144

Figure 1 LQFP144 Pinout



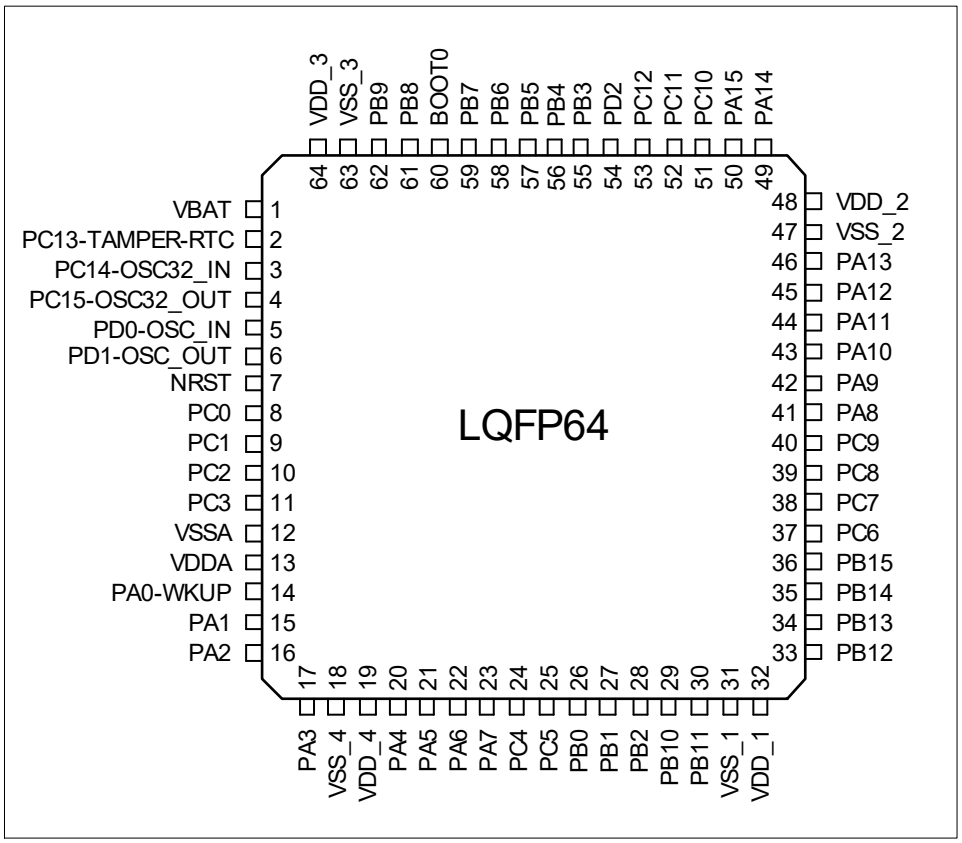
4.1.2 APM32F103xDxE Performance line LQFP100

Figure 2 LQFP100 Pinout



4.1.3 APM32F103xDxE Performance line LQFP64

Figure 3 LQFP64 Pinout



4.2 Pin Description

Table 8 APM32F103xDxE Pin Definitions

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
PE2	-	1	1	I/O	FT	PE2	TRACECK, SMC_A23	-
PE3	-	2	2	I/O	FT	PE3	TRACED0, SMC_A19	-
PE4	-	3	3	I/O	FT	PE4	TRACED1, SMC_A20	-
PE5	-	4	4	I/O	FT	PE5	TRACED2, SMC_A21	-
PE6	-	5	5	I/O	FT	PE6	TRACED3, SMC_A22	-
V_{BAT}	1	6	6	S	-	V_{BAT}	-	-
PC13- TAMPER-RTC (4)	2	7	7	I/O	-	PC13 (5)	TAMPER-RTC	-
PC14- OSC32_IN (4)	3	8	8	I/O	-	PC14 (5)	OSC32_IN	-
PC15- OSC32_OUT (4)	4	9	9	I/O	-	PC15 (5)	OSC32_OUT	-
PF0	-	-	10	I/O	FT	PF0	SMC_A0, DMC_A0	-
PF1	-	-	11	I/O	FT	PF1	SMC_A1, DMC_A1	-
PF2	-	-	12	I/O	FT	PF2	SMC_A2, DMC_A2	-
PF3	-	-	13	I/O	FT	PF3	SMC_A3, DMC_A3	-
PF4	-	-	14	I/O	FT	PF4	SMC_A4, DMC_A4	-
PF5	-	-	15	I/O	FT	PF5	SMC_A5, DMC_A5	-
V_{SS_5}	-	10	16	S	-	V_{SS_5}	-	-
V_{DD_5}	-	11	17	S	-	V_{DD_5}	-	-
PF6	-	-	18	I/O	-	PF6	ADC3_IN4, SMC_NIORD	-
PF7	-	-	19	I/O	-	PF7	ADC3_IN5,	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
							SMC_NREG	
PF8	-	-	20	I/O	-	PF8	ADC3_IN6, SMC_NIOWR	-
PF9	-	-	21	I/O	-	PF9	ADC3_IN7, SMC_CD	-
PF10	-	-	22	I/O	-	PF10	ADC3_IN8, SMC_INTR	-
OSC_IN	5	12	23	I	-	OSC_IN	-	PD0(7)
OSC_OUT	6	13	24	O	-	OSC_OUT	-	PD1(7)
NRST	7	14	25	I/O	-	NRST	-	-
PC0	8	15	26	I/O	-	PC0	ADC123_IN10, DMC_WE	-
PC1	9	16	27	I/O	-	PC1	ADC123_IN11, DMC_RAS	-
PC2	10	17	28	I/O	-	PC2	ADC123_IN12, DMC_CS	-
PC3	11	18	29	I/O	-	PC3	ADC123_IN13, DMC_CKE	-
V_{SSA}	12	19	30	S	-	V_{SSA}	-	-
V_{REF-}	-	20	31	S	-	V_{REF-}	-	-
V_{REF+}	-	21	32	S	-	V_{REF}+	-	-
V_{DDA}	13	22	33	S	-	V_{DDA}	-	-
PA0-WKUP	14	23	34	I/O	-	PA0	WKUP, USART2_CTS(6), ADC123_IN0, TMR2_CH1_ETR(6), TMR5_CH1, TMR8_ETR	-
PA1	15	24	35	I/O	-	PA1	USART2_RTS(6), ADC123_IN1, TMR5_CH2, TMR2_CH2(6)	-
PA2	16	25	36	I/O	-	PA2	USART2_TX(6), TMR5_CH3, ADC123_IN2, TMR2_CH3(6)	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
PA3	17	26	37	I/O	-	PA3	USART2_RX(6), TMR5_CH4, ADC123_IN3, TMR2_CH4(6)	-
V_{SS_4}	18	27	38	S	-	V_{SS_4}	-	-
V_{DD_4}	19	28	39	S	-	V_{DD_4}	-	-
PA4	20	29	40	I/O	-	PA4	SPI1_NSS(6), USART2_CK(6), DAC_OUT1, ADC12_IN4	-
PA5	21	30	41	I/O	-	PA5	SPI1_SCK(6), DAC_OUT2, ADC12_IN5	-
PA6	22	31	42	I/O	-	PA6	SPI1_MISO(7), TMR8_BKIN, ADC12_IN6 TMR3_CH1(7)	TMR1_BKIN
PA7	23	32	43	I/O	-	PA7	SPI1_MOSI(7) TMR8_CH1N ADC12_IN7 TMR3_CH2(7)	TMR1_CH1N
PC4	24	33	44	I/O	-	PC4	ADC12_IN14	-
PC5	25	34	45	I/O	-	PC5	ADC12_IN15	-
PB0	26	35	46	I/O	-	PB0	ADC12_IN8 TMR3_CH3 TMR8_CH2N	TMR1_CH2N
PB1	27	36	47	I/O	-	PB1	ADC12_IN9, TMR3_CH4(6) TMR8_CH3N	TMR1_CH3N
PB2	28	37	48	I/O	FT	PB2, BOOT1	-	-
PF11	-	-	49	I/O	FT	PF11	SMC_NIOS16	-
PF12	-	-	50	I/O	FT	PF12	SMC_A6, DMC_A6	-
V_{SS_6}	-	-	51	S	-	V_{SS_6}	-	-
V_{DD_6}	-	-	52	S	-	V_{DD_6}	-	-
PF13	-	-	53	I/O	FT	PF13	SMC_A7,	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
							DMC_A7	
PF14	-	-	54	I/O	FT	PF14	SMC_A8, DMC_A8	-
PF15	-	-	55	I/O	FT	PF15	SMC_A9, DMC_A9	-
PG0	-	-	56	I/O	FT	PG0	SMC_A10, DMC_A10	-
PG1	-	-	57	I/O	FT	PG1	SMC_A11, DMC_A11	-
PE7	-	38	58	I/O	FT	PE7	SMC_D4, DMC_D4	TMR1_ETR
PE8	-	39	59	I/O	FT	PE8	SMC_D5, DMC_D5	TMR1_CH1N
PE9	-	40	60	I/O	FT	PE9	SMC_D6, DMC_D6	TMR1_CH1
V_{SS_7}	-	-	61	S	-	V_{SS_7}	-	-
V_{DD_7}	-	-	62	S	-	V_{DD_7}	-	-
PE10	-	41	63	I/O	FT	PE10	SMC_D7, DMC_D7	TMR1_CH2N
PE11	-	42	64	I/O	FT	PE11	SMC_D8, DMC_D8	TMR1_CH2
PE12	-	43	65	I/O	FT	PE12	SMC_D9, DMC_D9	TMR1_CH3N
PE13	-	44	66	I/O	FT	PE13	SMC_D10, DMC_D10	TMR1_CH3
PE14	-	45	67	I/O	FT	PE14	SMC_D11, DMC_D11	TMR1_CH4
PE15	-	46	68	I/O	FT	PE15	SMC_D12, DMC_D12	TMR1_BKIN
PB10	29	47	69	I/O	FT	PB10	I2C2_SCL, I2C4_SCL, USART3_TX(6)	TMR2_CH3
PB11	30	48	70	I/O	FT	PB11	I2C2_SDA, I2C4_SDA, USART3_RX(6)	TMR2_CH4
V_{SS_1}	31	49	71	S	-	V_{SS_1}	-	-
V_{DD_1}	32	50	72	S	-	V_{DD_1}	-	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
PB12	33	51	73	I/O	FT	PB12	SPI2_NSS, I2S2_WS, I2C2_SMBAI, USART3_CK(6), TMR1_BKIN(6)	-
PB13	34	52	74	I/O	FT	PB13	SPI2_SCK, I2S2_CK, USART3_CTS(6), TMR1_CH1N	-
PB14	35	53	75	I/O	FT	PB14	SPI2_MISO, TMR1_CH2N, USART3_RTS(6)	-
PB15	36	54	76	I/O	FT	PB15	SPI2_MOSI, I2S2_SD, TMR1_CH3N(6)	-
PD8	-	55	77	I/O	FT	PD8	SMC_D13, DMC_D13	USART3_TX
PD9	-	56	78	I/O	FT	PD9	SMC_D14, DMC_D14	USART3_RX
PD10	-	57	79	I/O	FT	PD10	SMC_D15, DMC_D15	USART3_CK
PD11	-	58	80	I/O	FT	PD11	SMC_A16, DMC_BA0	USART3_CTS
PD12	-	59	81	I/O	FT	PD12	SMC_A17, DMC_BA1	TMR4_CH1, USART3_RTS
PD13	-	60	82	I/O	FT	PD13	SMC_A18	TMR4_CH2
V_{SS_8}	-	-	83	S	-	V_{SS_8}	-	-
V_{DD_8}	-	-	84	S	-	V_{DD_8}	-	-
PD14	-	61	85	I/O	FT	PD14	SMC_D0, DMC_D0	TMR4_CH3
PD15	-	62	86	I/O	FT	PD15	SMC_D1, DMC_D2	TMR4_CH4
PG2	-	-	87	I/O	FT	PG2	SMC_A12, DMC_A12	-
PG3	-	-	88	I/O	FT	PG3	SMC_A13, DMC_A13	-
PG4	-	-	89	I/O	FT	PG4	SMC_A14,	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
							DMC_A14	
PG5	-	-	90	I/O	FT	PG5	SMC_A15, DMC_A15	-
PG6	-	-	91	I/O	FT	PG6	SMC_INT2	-
PG7	-	-	92	I/O	FT	PG7	SMC_INT3	-
PG8	-	-	93	I/O	FT	PG8	DMC_CLK	-
V_{SS_9}	-	-	94	S	-	V_{SS_9}	-	-
V_{DD_9}	-	-	95	S	-	V_{DD_9}	-	-
PC6	37	63	96	I/O	FT	PC6	I2S2_MCK, TMR8_CH1, SDIO_D6	TMR3_CH1
PC7	38	64	97	I/O	FT	PC7	I2S3_MCK, TMR8_CH2, SDIO_D7	TMR3_CH2
PC8	39	65	98	I/O	FT	PC8	TMR8_CH3, SDIO_D0	TMR3_CH3
PC9	40	66	99	I/O	FT	PC9	TMR8_CH4, SDIO_D1	TMR3_CH4
PA8	41	67	100	I/O	FT	PA8	USART1_CK, TMR1_CH1(6), MCO	-
PA9	42	68	101	I/O	FT	PA9	USART1_TX(6), TMR1_CH2(6)	-
PA10	43	69	102	I/O	FT	PA10	USART1_RX(6), TMR1_CH3(6)	-
PA11	44	70	103	I/O	FT	PA11	USART1_CTS, USBDDM, USBD2DM, CAN_RX(6), TMR1_CH4(6)	-
PA12	45	71	104	I/O	FT	PA12	USART1_RTS, USBDDP USBD2DP, CAN_TX(6), TMR1_ETR(6)	-
PA13	46	72	105	I/O	FT	JTMS/	-	PA13

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
						SWDIO		
-	-	73	106	-	-	-	-	-
V_{SS_2}	47	74	107	S	-	V_{SS_2}	-	-
V_{DD_2}	48	75	108	S	-	V_{DD_2}	-	-
PA14	49	76	109	I/O	FT	JTCK/ SWCLK	-	PA14
PA15	50	77	110	I/O	FT	JTDI	SPI3_NSS, I2S3_WS	TMR2_CH1_ETR, PA15, SPI1_NSS
PC10	51	78	111	I/O	FT	PC10	UART4_TX, SDIO_D2	USART3_TX
PC11	52	79	112	I/O	FT	PC11	UART4_RX, SDIO_D3	USART3_RX
PC12	53	80	113	I/O	FT	PC12	UART5_TX, SDIO_CK	USART3_CK
PD0	-	81	114	I/O	FT	OSC_IN (7)	SMC_D2, DMC_D2	CAN_RX
PD1	-	82	115	I/O	FT	OSC_OUT (7)	SMC_D3, DMC_D3	CAN_TX
PD2	54	83	116	I/O	FT	PD2	TMR3_ETR, UART5_RX, SDIO_CMD	-
PD3	-	84	117	I/O	FT	PD3	SMC_CLK	USART2_CTS
PD4	-	85	118	I/O	FT	PD4	SMC_NOE	USART2_RTS
PD5	-	86	119	I/O	FT	PD5	SMC_NWE	USART2_TX
V_{SS_10}	-	-	120	S	-	V_{SS_10}	-	-
V_{DD_10}	-	-	121	S	-	V_{DD_10}	-	-
PD6	-	87	122	I/O	FT	PD6	SMC_NWAIT	USART2_RX
PD7	-	88	123	I/O	FT	PD7	SMC_NE1, SMC_NCE2	USART2_CK
PG9	-	-	124	I/O	FT	PG9	SMC_NE2, SMC_NCE3	-
PG10	-	-	125	I/O	FT	PG10	SMC_NCE4_1, SMC_NE3	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
PG11	-	-	126	I/O	FT	PG11	SMC_NCE4_2	-
PG12	-	-	127	I/O	FT	PG12	SMC_NE4	-
PG13	-	-	128	I/O	FT	PG13	SMC_A24	-
PG14	-	-	129	I/O	FT	PG14	SMC_A25	-
V_{SS_11}	-	-	130	S	-	V_{SS_11}	-	-
V_{DD_11}	-	-	131	S	-	V_{DD_11}	-	-
PG15	-	-	132	I/O	FT	PG15	DMC_CAS	-
PB3	55	89	133	I/O	FT	JTDO	SPI3_SCK, I2S3_CK	PB3, TRACESWO, TMR2_CH2, SPI1_SCK
PB4	56	90	134	I/O	FT	NJTRST	SPI3_MISO	PB4, TMR3_CH1, SPI1_MISO
PB5	57	91	135	I/O	-	PB5	I2C1_SMBAI, SPI3_MOSI, I2S3_SD	TMR3_CH2, SPI1_MOSI
PB6	58	92	136	I/O	FT	PB6	I2C1_SCL(6), I2C3_SCL, TMR4_CH1(6)	USART1_TX
PB7	59	93	137	I/O	FT	PB7	I2C1_SDA(6), I2C3_SDA, SMC_NADV , TMR4_CH2(6)	USART1_RX
BOOT0	60	94	138	I	-	BOOT0	-	-
PB8	61	95	139	I/O	FT	PB8	TMR4_CH3(6), SDIO_D4	I2C1_SCL, I2C3_SCL, CAN_RX
PB9	62	96	140	I/O	FT	PB9	TMR4_CH4(6) SDIO_D5	I2C1_SDA, I2C3_SDA, CAN_TX
PE0	-	97	141	I/O	FT	PE0	TMR4_ETR, SMC_NBL0, DMC_LDQM	-
PE1	-	98	142	I/O	FT	PE1	SMC_NBL1, DMC_UDQM	-
V_{SS_3}	63	99	143	S	-	V_{SS_3}	-	-

Pin Name	Pins			Type (1)	I/O level (2)	Main Function (3)	Alternate functions	
	LQFP64	LQFP100	LQFP144			(after reset)	Default	Remap
V_{DD_3}	64	100	144	S	-	V_{DD_3}	-	-

(1) I = input, O = output, S = supply, HiZ = high resistance

(2) FT = 5V tolerant.

(3) Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively.

(4) PC13, PC14 and PC15 are supplied through the power switch since the switch only sinks a limited amount of current (3mA). The use of GPIOs from PC13 to PC15 in output mode is limited: only one GPIO can be used at a Time, the speed should not exceed 2 MHz with a maximum load of 30pF and these IOs must not be used as a current source (e.g. to drive an LED).

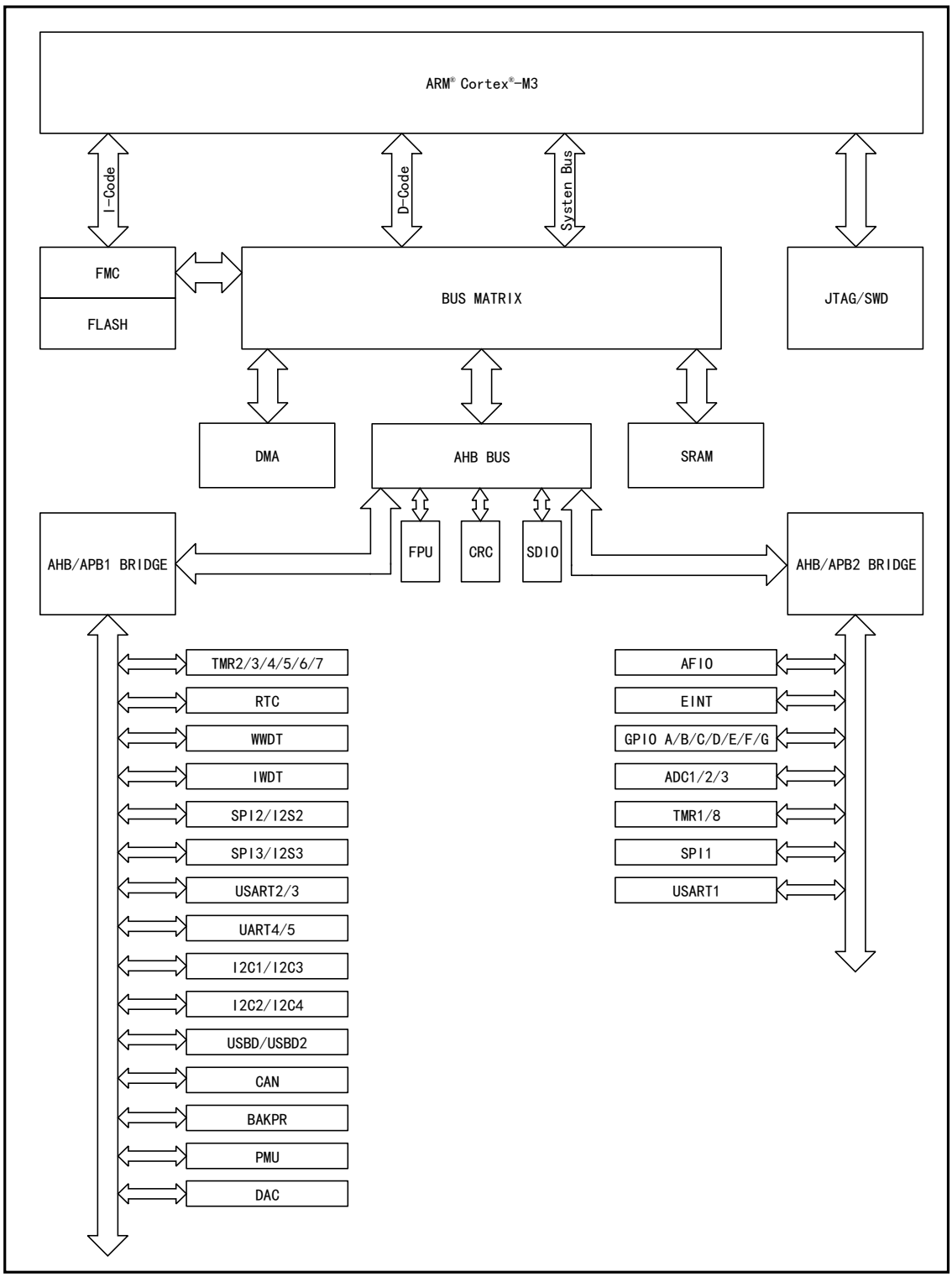
(5) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BAKPR register description sections in the reference manual.

(6) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual.

(7) Pin5 and pin6 in the LQFP64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate Function I/O and Debug Configuration section in the reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

5 System Diagram

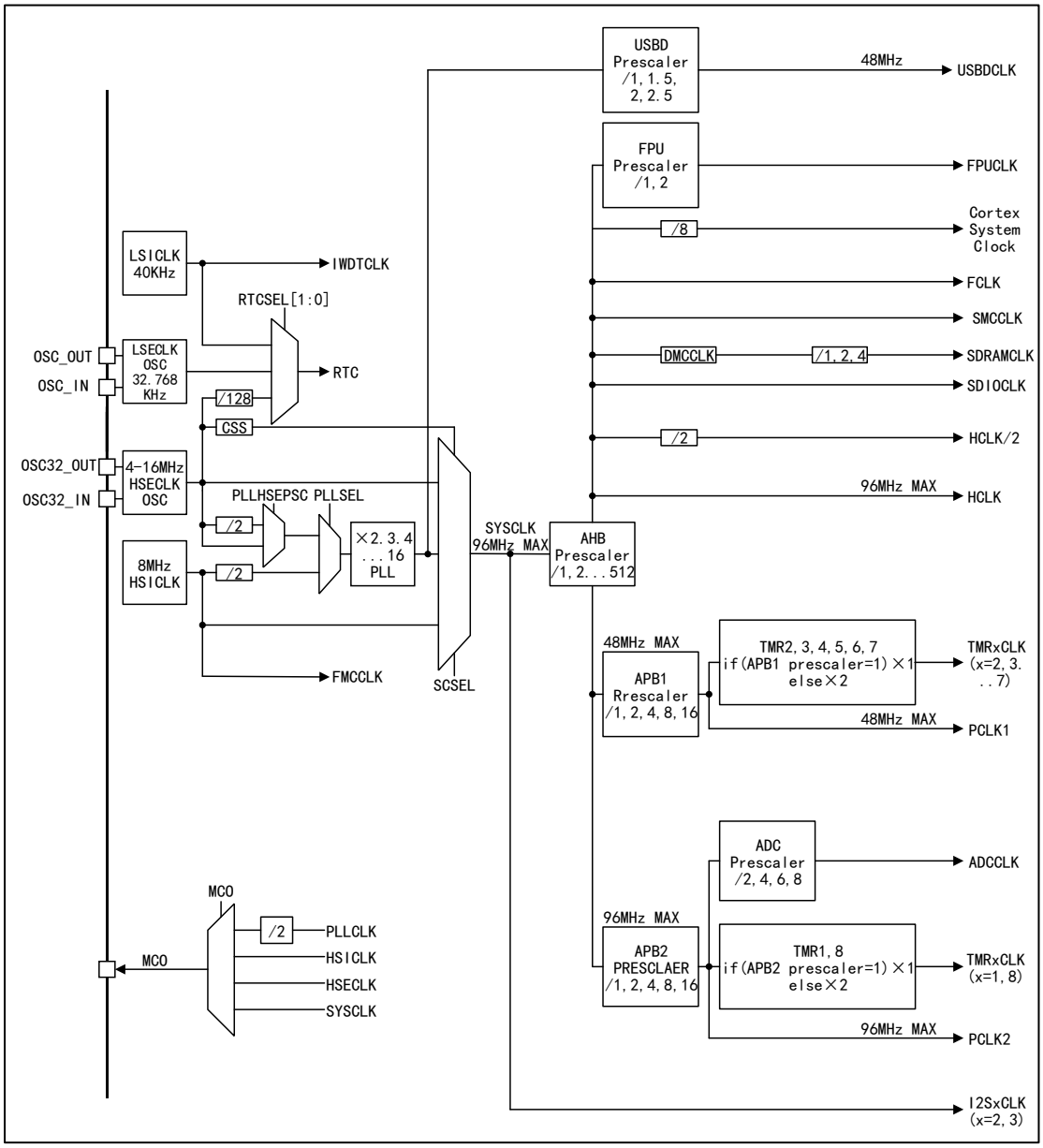
Figure 4 APM32F103xDxE Performance Line System Diagram



1. Operating temperature: -40°C to +85°C（suffix 6）or -40°C to +105°C（suffix7）, junction temperature up to 105°C.
2. AF: Alternate function on I/O port pin.

6 Clock Tree

Figure 5 APM32F103xDxE Performance Line Clock Tree

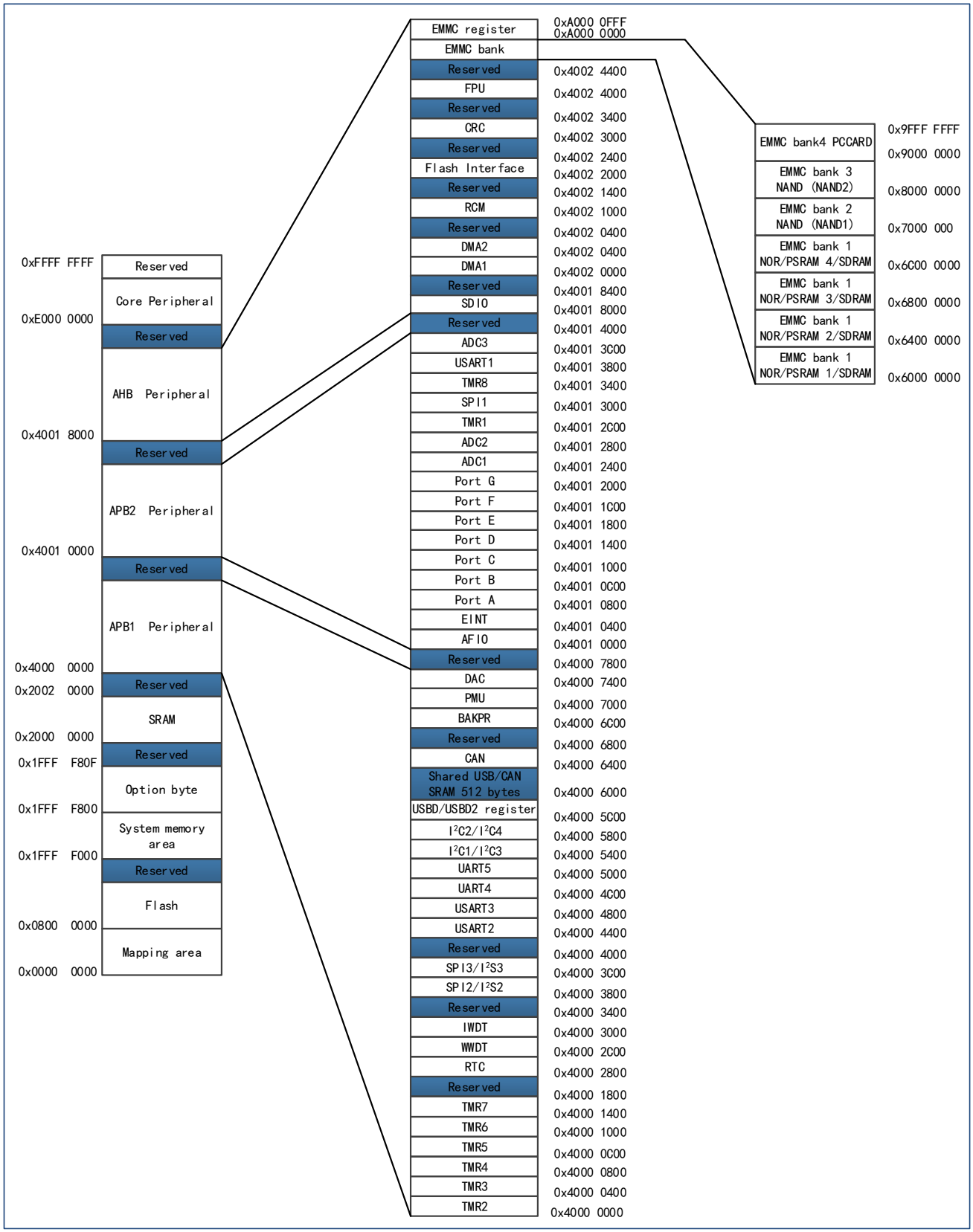


1. For the USBD function to be available, both HSECLK and PLL must be enabled, with the USBDCLK at 48 MHz.

2. To have an ADC conversion time of 1μs, APB2 must be at 14 MHz, 28MHz or 56MHz.

7 Address Mapping

Figure 6 APM32F103xDxE Performance Line Address Mapping Diagram



Note: SDRAM is directly addressed to 256M, without Bank access separately.

8 Electrical Characteristics

8.1 Parameter Conditions

All voltage parameters are referenced to V_{SS} unless otherwise specified.

8.1.1 Maximum and Minimum Values

Unless otherwise stated, all minimum and maximum values are guaranteed on the production line by testing 100% of the product at ambient temperature T_A=25°C and T_A=$T_A$max under worst ambient temperature, supply voltage and clock frequency conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3∑).

8.1.2 Typical Value

Typical data is based on T_A =25°C and V_{DD} =3.3V (2 V ≤ V_{DD} ≤ 3.3 V voltage range) unless otherwise stated. These data are for design guidance only.

8.1.3 Typical Curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

8.1.4 Loading Capacitor

Figure 7 Load conditions when measuring pin parameters

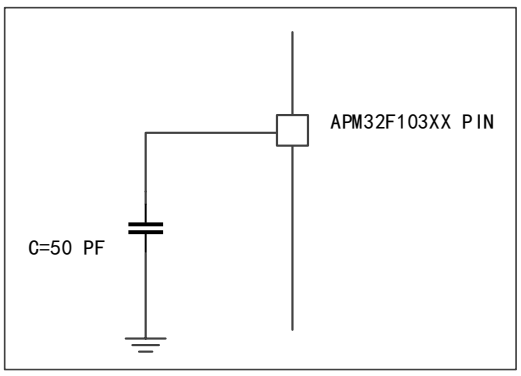


Figure 8 Pin Input Voltage Measurement Scheme

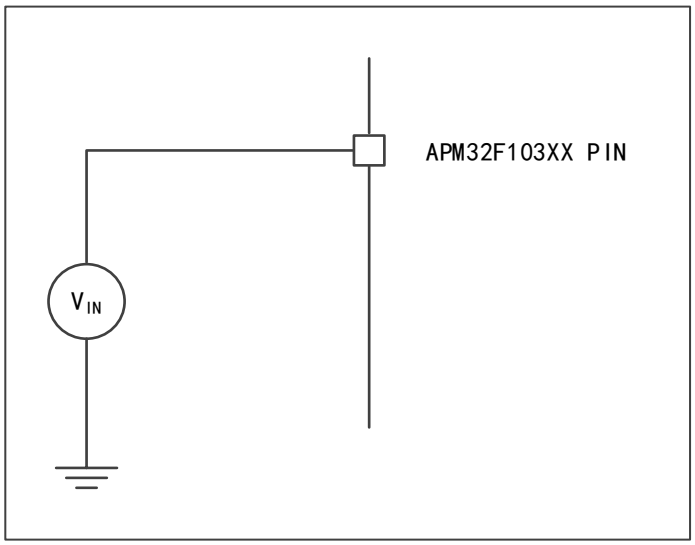
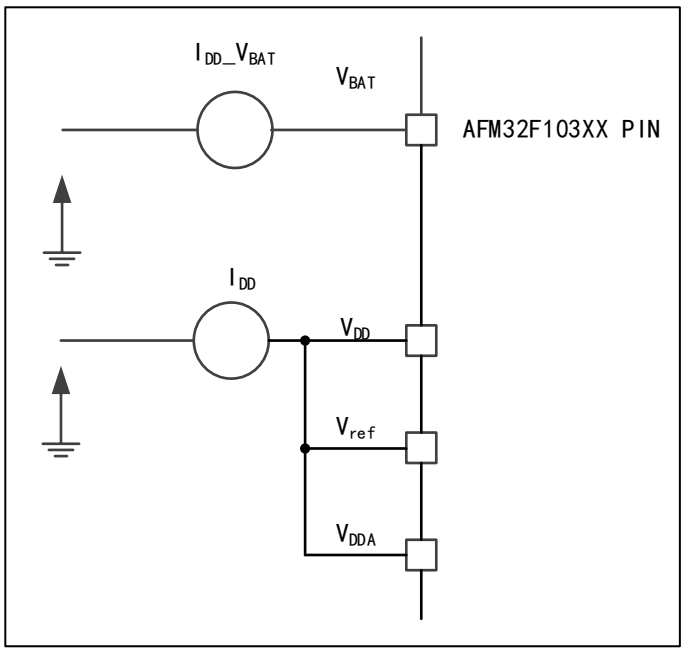
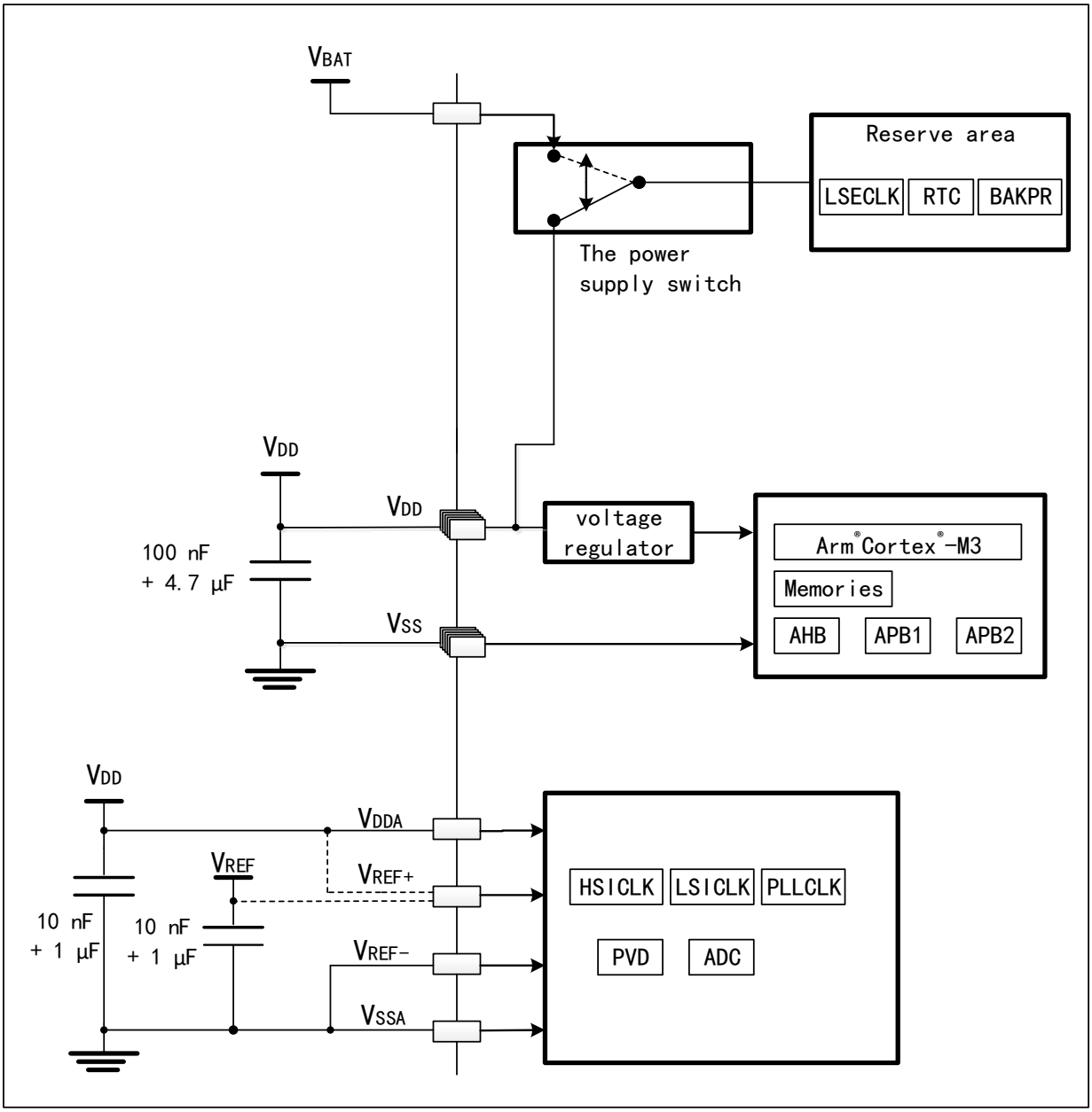


Figure 9 Current Consumption Measurement Scheme



8.1.5 Power supply scheme

Figure 10 Power supply scheme



8.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 9 :Maximum rated voltage characteristics and Table 10: Maximum rated current characteristics may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

8.2.1 Maximum Rated Voltage Characteristics

Table 9 Maximum rated voltage characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{DD}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins (2)	V_{SS}-0.3	5.5	
	Input voltage on other pins(2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins		50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different ground pins		50	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to a power supply within the external allowable range.
2. If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When V_{IN} > V_{DD}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current.

8.2.2 Maximum Rated Current Characteristics

Table 10 Maximum rated current characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current (supply current) (1) went through the V_{DD}/V_{DDA} power cord.	150	mA
I_{VSS}	Total current (outflow current) (1) went through the V_{SS} ground cord.	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2) (3)	Injection current of NRST pin	±5	
	Injection current of HSECLK's OSC_IN pin and LSECLK's OSC_IN pin	±5	
	Injection current of other pins	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (4)	±25	

1. All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to a power supply within the external allowable range.
2. If V_{IN} does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If VIN exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When V_{IN} > V_{DD}, there is a forward injection current; when V_{IN} < V_{SS}, there is a reverse injection current.
3. Reverse injection current can interfere with the analog performance of the ADC.
4. When several I/O ports have injection current at the same time, the maximum value of$\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of $\Sigma I_{INJ(PIN)}$ on the four I/O port pins of the device.

8.2.3 Maximum Temperature Characteristics

Table 11 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-55 ~ + 150	°C
T_J	Maximum junction temperature	150	°C

8.3 Testing Under General Operating Conditions

Table 12 General Operating Conditions

Symbol	Parameters	Conditions	Min value	Max value	Unit
f_{HCLK}	Internal AHB clock frequency		0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	
f_{PCLK2}	Internal APB2 clock frequency		0	96	
V_{DD}	Standard working voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	must be the same with V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC not used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V
T_A	Ambient temperature range (temperature label 7)	Maximum power consumption	-40	105	°C
T_J	Junction temperature range		-40	150	°C

1. When the ADC is used, refer to Chapter 8.3.13
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

8.3.1 Embedded Reset and Power Control Block Characteristics (1)

Table 13 Embedded Reset and Power Control Block Characteristics (-40°C < T_A < +105°C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{PVD}(3)	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.16	2.19	2.22	V
		PLS[2:0]=000 (falling edge)	2.06	2.09	2.11	V
		PLS[2:0]=001 (rising edge)	2.26	2.29	2.32	V
		PLS[2:0]=001 (falling edge)	2.15	2.18	2.21	V
		PLS[2:0]=010 (rising edge)	2.36	2.39	2.42	V
		PLS[2:0]=010 (falling edge)	2.25	2.28	2.31	V
		PLS[2:0]=011 (rising edge)	2.45	2.49	2.52	V
		PLS[2:0]=011 (falling edge)	2.35	2.38	2.41	V
		PLS[2:0]=100 (rising edge)	2.55	2.59	2.62	V
		PLS[2:0]=100 (falling edge)	2.44	2.48	2.51	V
		PLS[2:0]=101 (rising edge)	2.65	2.68	2.72	V
		PLS[2:0]=101 (falling edge)	2.55	2.58	2.61	V
		PLS[2:0]=110 (rising edge)	2.75	2.79	2.82	V
		PLS[2:0]=110 (falling edge)	2.64	2.67	2.71	V
		PLS[2:0]=111 (rising edge)	2.84	2.88	2.92	V
		PLS[2:0]=111 (falling edge)	2.74	2.78	2.81	V
$V_{PVDhyst}$(2)	PVD hysteresis			107.08		mV
$V_{POR/PDR}$	Power on/power down reset threhold	Falling edge	1.86(1)	1.88	1.90	V
		Rising edge	1.91	1.94	1.96	V
$V_{PDRhyst}$ (2)	PVD hysteresis		38.19	55.33	72.47	mV
$T_{RSTTEMPO}$	Reset Duration			1.47		ms

(1) The product feature is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

(2) It is guaranteed by design, and is not tested in production.

(3) It is derived from a comprehensive evaluation and is not tested in production.

8.3.2 Embedded Reference Voltage Characteristics Test

Table 14 Embedded Reference Voltage

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REFINT}(1)	Internal reference voltage	-40°C < T_A < +105°C	1.17	1.21	1.27	V

		V_{DD}= 2-3.6 V				
$T_{S\_vrefint}$(2)	ADC sampling time when reading the internal reference voltage			5.1	17.1	μs
V_{REFINT}(2)	Internal reference voltage spread over the temperature range	V_{DD}=3V±10mV	-	-	18	mV
T_{Coeff}	Temperature coefficient	-			104	ppm/℃

1. It is derived from a comprehensive evaluation and is not tested in production.
2. It is guaranteed by design, and is not tested in production.

8.3.3 Supply Current Characteristics

The current values in the operating modes given in this section are measured by executing Dhrystone 2.1, with the Keil V5 compilation environment and the L0 compilation optimization level.

Max Current Consumption

MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise stated.
- The flash memory access time is adjusted to the f_{HCMU} frequency (0 wait state from 0 ~ 24 MHz, 1 wait state from 24~ 48 MHz, 2 wait states from 48 ~72 MHz, 3 wait states from 72 ~ 96 MHz).
- Prefetch in ON (tip: this bit must be set before the clock setting and bus prescaling).
- When the peripherals are enabled: $fp_{CMU1} = f_{HCMU}/2$, $fp_{CMU2} = f_{HCMU}$.

Table 15 Maximum current consumption in Run mode, data process code run from Flash

Symbol	Parameter	Conditions	f_{HCMU}	Maximum Value(1)	Unit
				T_A=105°C , V_{DD}=3.6 V	
I_{DD}	Supply current in run mode	External clock (2), all peripherals enabled	96 MHz	48.9	mA
			72MHz	34.5	
			48MHz	27.6	
			36MHz	21.6	
			24MHz	15.2	
			16MHz	10.7	
			8MHz	6.2	
		External clock (2), all peripherals disabled	96 MHz	27.0	
			72MHz	26.9	
			48MHz	16.9	
			36MHz	13.3	
			24MHz	9.71	
			16MHz	7.10	
			8MHz	4.35	

1. It is derived from a comprehensive evaluation and is not tested in production.

2. External clock is 8 MHz and PLL is on when f_{HCMU} > 8 MHz.

Table 16 Maximum current consumption in Run mode, data process code run from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Maximum Value(1)	Unit
				TA =105°C , VDD=3.6 V	
I_{DD}	Supply current in run mode	External clock (2), all peripherals enabled	96 MHz	40.7	mA
			72MHz	32.1	
			48MHz	20.9	
			36MHz	16.6	
			24MHz	11.4	
			16MHz	8.17	
			8MHz	3.87	
		External clock (2), all peripherals disabled	96 MHz	26.5	
			72MHz	20.5	
			48MHz	14.5	
			36MHz	11.3	
			24MHz	8.22	
			16MHz	6.10	
			8MHz	3.88	

1. It is derived from a comprehensive evaluation and is not tested in production.

2.External clock is 8 MHz and PLL is on when f_{HCMU} > 8 MHz.

Table 17 Maximum current consumption in Sleep mode, data process code run from Flash or RAM

Symbol	Parameters	Conditions	f_{HCLK}	Maximum Value(1)	Unit
				TA =105°C , VDD=3.6 V	
I_{DD}	Supply current in sleep mode	External clock (2), all peripherals enabled	96 MHz	34.4	mA
			72MHz	23.7	
			48MHz	18.6	
			36MHz	14.7	
			24MHz	10.5	
			16MHz	7.88	
			8MHz	5.05	
		External clock (2), all peripherals disabled	96 MHz	8.38	
			72MHz	6.32	
			48MHz	5.35	
			36MHz	4.64	
			24MHz	4.03	
			16MHz	3.55	
			8MHz	2.91	

1. It is derived from a comprehensive evaluation and is not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCMU} > 8 MHz.

Table 18 Maximum Current Consumption in Stop Mode and Standby Mode

Symbol	Parameter	Conditions	Maximum Value(1) T_A=105°C，VDD=3.6 V	Unit
I_{DD}	Supply current in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	413.31	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	390.95	
	Supply current in standby mode	Low-speed internal RC oscillator and independent watchdog ON	25.44	
		Low-speed internal RC oscillator is on, independent watchdog OFF	22.73	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	21.75	
I_{DD_VBAT}	Supply current in the backup area	Low-speed oscillator and RTC ON	4	

1. It is derived from a comprehensive evaluation and is not tested in production.

Typical Current Consumption

MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The flash memory access time is adjusted to the f_{HCMU} frequency (0 wait state from 0 ~ 24 MHz, 1 wait state from 24~48 MHz, 2 wait states from 48~72 MHz, 3 wait states from 72~96 MHz).
- Prefetch in ON (tip: this bit must be set before the clock setting and bus prescaling).

When the peripherals are enabled: $f_{PCLK1}=F_{HCLK}/2$，$f_{pCLK2}=f_{HCLK}$。

Table 19 Typical current consumption in Run mode, data process code run from Flash

Symbol	Parameter	f_{HCMU}	Typical Value(1)		Unit
			T_A=25°C,V_{DD}=3.3V		
			External clock(2), all peripherals enabled	External clock(2), all peripherals disabled	
I_{DD}	Supply current in run mode	96 MHz	45.6	25.7	mA
		72MHz	32.9	19.4	
		48MHz	26.2	16.0	
		36MHz	20.1	12.5	
		24MHz	14.5	9.30	
		16MHz	10.1	6.68	
		8MHz	5.77	4.04	

1. It derived from comprehensive evaluation and is not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCMU} > 8 MHz.

Table 20 Typical current consumption in Run mode, c data process code run from RAM

Symbol	Parameter	f_{HCMU}	Typical Value(1)		Unit
			T_A=25°C,V_{DD}=3.3V		
			External clock(2), all peripherals enabled	External clock(2), all peripherals disabled	
I_{DD}	Supply current in run mode	96 MHz	37.5	25.2	mA
		72MHz	28.6	19.5	
		48MHz	19.8	13.6	
		36MHz	15.4	10.7	
		24MHz	10.6	7.52	
		16MHz	7.68	5.63	
		8MHz	3.57	3.58	

1. It derived from comprehensive evaluation and is not tested in production.
2. When the external clock is 8MHz and f_{HCMU} >8MHz, it enables PLL.

Table 21 Typical current consumption in sleep mode, code run from Flash or RAM

Symbol	Parameter	f_{HCMU}	Typical Value(1)		Unit
			T_A=25°C,V_{DD}=3.3V		
			External clock(2), all peripherals enabled	External clock(2), all peripherals disabled	
I_{DD}	Supply current in sleep mode	96 MHz	31.2	7.08	mA
		72MHz	21.5	5.24	
		48MHz	16.6	4.31	
		36MHz	12.6	3.64	
		24MHz	8.95	2.99	
		16MHz	6.57	2.53	
		8MHz	4.01	1.97	

1. It derived from comprehensive evaluation and is not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCMU} > 8 MHz.

Table 22 Typical current Consumption in Stop Mode and Standby Mode

Symbol	Parameters	Conditions	Typical Value(TA =25°C)		Unit
			VDD= 2.4V	VDD= 3.3V	
IDD	Supply current in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	28.9	28.3	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	16.8	18.5	
	Supply current in standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.69	4.01	
		Low-speed internal RC oscillator is on, independent watchdog OFF	2.69	3.83	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.23	3.13	
I_{DD_VBAT}	Supply current in the backup area	Low-speed oscillator and RTC ON		1.5	

8.3.4 External Clock Source Characteristics

Crystal/ceramic resonators generate high speed external clocks

High Speed External (HSECLK) clocks can be supplied with a 4 to 16MHz crystal/ceramic resonator oscillator.All information presented in this section is based on the results of a comprehensive feature evaluation of typical external components in Table 23.In applications, the resonator and load capacitors must be as close to the oscillator pin as possible to reduce output distortion and stabilization time at startup.

For detailed crystal resonator parameters (frequency, package, precision, etc.), please consult the appropriate manufacturer.

Table 23 HSECLK 4~16 MHz Oscillator Characteristics(1)(2)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{OSC_IN}	Oscillator Frequency:	-	4	8	16	MHz
R_F	Feedback Resistance	-	-	300	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (RS)(3)	R_S = 30kΩ	-	30	-	pF
i_2	HSECLK driving current	V_{DD}=3.3V，V_{IN}=V_{SS} 30pF load	-	-	1.1	mA
$t_{SU(HSECLK)}$(4)	Startup time	V_{DD} is stabllized	0.60	0.96	1.33	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. It is derived from a comprehensive evaluation and is not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSECLK)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Crystal/ceramic resonators generate low speed external clocks

The low-speed external(LSECLK) clock can be supplied with a 32.768 KHz crystal\ceramic resonator oscillator. All information given in this section are based on characterization results obtained with typical external components specified in *Table 24.* In the application, the resonator and the load capacitors have to be placed as closed as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 24 LSECLK oscillator characteristics (f_{LSECLK} = 32.768 kHz)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
f_{OSF_IN}	Oscillator Frequency:	-	-	32.768	-	KHz
RF	Feedback Resistance	-	-	7	-	MΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (RS)(3	R_S = 30kΩ			15	pF
i_2	LSECLK driving current	V_{DD}=3.3V， V_{IN}=V_{SS}			1.4	μA
$t_{SU(LSECLK)}$（4）	Startup time	T_A=105℃ or 25℃， V_{DD}= 2-3.6V	0.62	1.32	2.02	s
		T_A=25℃，V_{DD}=3.3V	0.47	1.17	1.86	
		T_A=-40℃，V_{DD}=3.3V	0.32	4.32	8.32	

(1) It is derived from a comprehensive evaluation and is not tested in production.

(2) Refer to the note and caution paragraphs below the table.

(3) $t_{SU(LSECLK)}$ is the starting time, which is measured from the software enabled LSECLK until a stable oscillation of 32.768kHz is obtained.This value is measured using a standard crystal resonator and may vary widely from crystal manufacturer to crystal manufacturer.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Table 23). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. Load capacitance CL has the following formula: C_L = C_{L1} x C_{L2} / (C_{L1} + C_{L2}) + Cstray where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.

8.3.5 Internal Clock Source Characteristics

High Speed Internal (HSICLK) RC Oscillator Test

Table 25 HSICLK Oscillator Features(1)

Symbol	Parameters	Conditions		Minimum Value	Typical Value	Maximum Value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
ACC_{HSICLK}	HSICLK oscillator accuracy	Factory calibrated	T_A=-25°C V_{DD} = 3.3V	-1	-	+1	%

			T_A=-40~105°C V_{DD} = 3.3V	-2.76	-	2.3	%
			T_A=-40~105°C V_{DD} = 2-3.6V	-2.76	-	2.45	%
$t_{SU(HSICLK)}$	HSICLK oscillator startup time	V_{DD} = 3.3V T_A =-40~105°C		1.68	-	1.78	μs

1. It is derived from a comprehensive evaluation and is not tested in production.

Low Speed Internal (LSICLK) Oscillator Test

Table 26 LSICLK Oscillator Characteristics (1)

Symbol	Parameters	Minimum Value	Typical Value	Maximum Value	Unit
f_{LSICLK}	Frequency (V_{DD} = 2-3.6V，T_A = -40~105°C)	30	41.50	60	KHz
$t_{SU(LSICLK)}$	LSICLK oscillator startup time (V_{DD} = 3.3V，T_A = -40~105°C)	-	-	43.33	μs

1. It is derived from a comprehensive evaluation and is not tested in production.

Wake Up Time from Low-power Mode

The time values in the table are measured during the wake phase by an 8MHz HSICLK oscillator as the wake clock source.The clock source used when waking up is determined by the current operating mode:

- Stop or standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock set before entering Sleep mode

Table 27 Wake Up time in Low-power Mode

Symbol	Parameter	Typical Value	Unit
$t_{WUSLEEP}$(1)	Wake up from Sleep mode	1.78	μs
t_{WUSTOP}(1)	Wake up from Stop mode (regulator in run mode)	2.55	μs
	Wakeup from Stop mode (regulator in low-power mode)	4.28	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	26.55	μs

1.The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

8.3.6 PLL Characteristics

Table 28 PLL Characteristics

Symbol	Parameters	Value			Unit
		Minimum Value	Typical Value	Maximum Value (1)	
f_{PLL_IN}	PLL Input clock (2)	1	8	25	MHz
	PLLInput Clock Duty Cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock (V_{DD} = 3.3V，T_A = -40~105°C）	2	-	96	MHz
t_{LOCK}	PLL lock time			112.21	μs

1. It is derived from a comprehensive evaluation and is not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

8.3.7 Memory Characteristics

FLASH Memory

Table 29 FLASH Memory Characteristics (1)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
t_{prog}	16-bit programming time	T_A = -40~105°C V_{DD}=2.4~3.6V	33.7	37.1	40.5	μs
t_{ERASE}	Page (1K bytes) erase time	T_A = -40~105°C V_{DD}=2.4~3.6V	3.50	3.11	3.50	ms
t_{ME}	Mass erase time	T_A = 25°C V_{DD}=3.3V	25.4	26.5	27.7	ms
V_{prog}	Programming voltage	T_A = -40~105°C	2.0	3.3	3.6	V

1. It is derived from a comprehensive evaluation and is not tested in production.

8.3.8 EMC Characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

- FTB: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Device reset allows normal operation to resume.

The test results are shown in Table 30.

Table 30 EMS Characteristics

Symbol	Parameters	Conditions	Level
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance.	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-2	2A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance.	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	3A

Designing hardened software to avoid noise problems

EMC characterization and optimization at component level were performed using typical application environments and simplified MCU software.It is important to note that good EMC performance is highly dependent on user applications, especially software.

Therefore, it is recommended that users implement EMC optimization for their software and conduct EMC-related certification testing.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J1752/3 standard which specifies the test board and the pin loading.

Table 31 EMI Characteristics

Symbol	Parameters	Conditions	Detection frequency band	Maximum value (f_{HSECLK}/f_{HCLK})		Unit
				8/48 MHz	8/72 MHz	
SEMI	Peak	V_{DD} = 3.3V，T_A = 25 °C, LQFP144 package compliant with SAE J1752/3	30~130 MHz	PASS	PASS	dBμV
			130 MHz ~1GHz	PASS	PASS	

8.3.9 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32 ESD Absolute maximum ratings

Symbol	Parameter	Conditions	Maximum Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = +25 °C, conforming to JESD22-C101	2000	

Static latch-up

Two complementary static bolt-lock tests are required on 6 samples to evaluate the bolt-lock performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 33 Static latch-up(1)

Symbol	Parameter	Conditions	Type
LU	Static latch-up	T_A = +25 °C/105°C conforming to EIA/JESD78E	±200mA

(1) the sample data is measured by other testing institutions, and no testing is conducted in production.

8.3.10 I/O Port Characteristics

Input/Output Static Characteristics

Table 34 I/O Static Characteristics (Test conditions V_{DD} = 2.7-3.6V, T_A = -40 ~ 105 ° C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IL}	Low level input voltage	TTL port	-0.5	-	0.8	V
V_{IH}	Standard I/O pin input high level voltage		2		V_{DD}+0.5	
	FT I/O pin(1), input high level voltage		2		5.5	
V_{IL}	Input low level voltage	CMOS port	-0.5		$0.3V_{DD}$	
V_{IH}	Input high level voltage		$0.7V_{DD}$		V_{DD}+0.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2))		150			mV
	I/OFT Schmitt trigger voltage hysteresis(2)		5% V_{DD}			mV
I_{lkg}	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port			±1	μA
		V_{IN} = 5V , I/O FT			1	
R_{PU}	Weak pull-up equivalent resistance(4)	$V_{IN} = V_{SS}$	32	40	49	kΩ
R_{PD}	Weak pull-down equivalent resistance (4)	$V_{IN} = V_{DD}$	32	40	49	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = 5V tolerant. In order to sustain a voltage higher than VDD+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. It is derived from a comprehensive evaluation and is not tested in production.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS.

Output Driving Current Test

The GPIO (General Purpose Input/Output Port) can sink or output up to ±8mA, and can sink up to ±20mA (V_{OL}/V_{OH} reduction). In user applications, the number of I/Os capable of driving current must be limited so that the current consumed cannot exceed the absolute maximum rating:

- The sum of the currents sourced by all the I/Os on V_{DD} plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents sunk by all the I/O on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output Voltage Test

Table 35 Output Voltage Characteristics (test conditions V_{CC}=2.7-3.6V, T_A = -40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port, I_{IO} = +8mA 2.7V < V_{DD} < 3.6V	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD} - 0.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port, I_{IO} = +8mA 2.7V < V_{DD} < 3.6V	-	0.4	V
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
$V_{OL}^{(1)(3)}$	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20mA 2.7V < V_{DD} < 3.6V	-	1.3	V
$V_{OH}^{(2)(3)}$	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD} - 1.3	-	

1. The IIO current sunk by the device must always respect the absolute maximum rating specified in, and the sum of IIO (I/O ports and control pins) must not exceed IVSS.

2. The IIO current sourced by the device must always respect the absolute maximum rating specified in, and the sum of IIO (I/O ports and control pins) must not exceed IVDD.

3. It is derived from a comprehensive evaluation and is not tested in production.

Input and Output AC Features (T_A = 25°C)

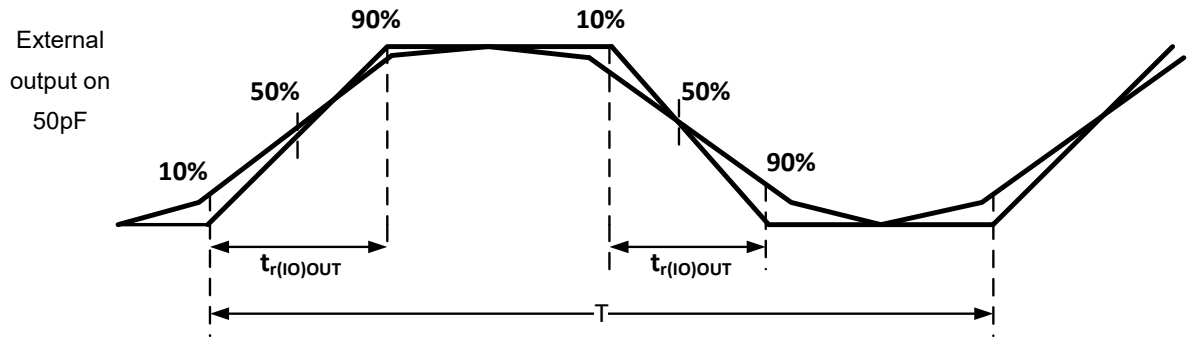
Table 36 I/O AC Characteristics

MODEx[1:0] Configuration	Symbol	Parameters	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency$^{(2)}$	C_L = 50 pF, V_{DD} = 2~3.6V		2	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L = 50 pF, V_{DD} = 2~3.6V		50$^{(3)}$	ns

	$t_{r\ (IO)out}$	Output low to high rise time			50(3)	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2~3.6V		10	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L = 50 pF, V_{DD} = 2~3.6V		24(3)	ns
	$t_{r\ (IO)out}$	Output low to high rise time			23	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7~3.6V		48	MHz
	$t_{f(IO)out}$	Output high to low fall time	C_L = 30 pF, V_{DD} = 2.7~3.6V		7(3)	ns
	$t_{r\ (IO)out}$	Output low to high rise time			5(3)	

1. The I/O speed can be configured by MODEx[1:0].
2. The maximum frequency is defined in the figure below.
3. It is guaranteed by design and is not tested n production.

Figure 11 I/O AC Characteristics Definition



Maximum frequency is achieved if $t_r + t_f \leq (2/3)T$ and if the duty cycle is (45~55%) when loaded by 50pF

8.3.11 NRST Pins Characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Table 37 NRST Pin Characteristics (Test condition V_{CC}=3.3V, T_A = -40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	

$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	270	300	340	mV
R_{PU}	Weak pull-up equivalent resistance(2)	$V_{IN} = V_{SS}$	30	40	53	kΩ

1. It is guaranteed by design, and is not tested in production.
2. The pull-up resistor is implemented by a pure resistor in series with a switchable PMOS/NMOS transistor. The PMOS/NMOS switch has a small resistance.

8.3.12 Communication Interface

I²C Interface Characteristics

Table 38 I²C Interface Characteristics (Test conditions V_{DD}=3.3V, T_A = 25°C)

Symbol	Parameters	Standard I²C(1)		Fast I²C(1) (2)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	
$t_{w(SCLL)}$	SCL clock low time	4.88	-	1.77	-	μs
$t_{w(SCLH)}$	SCL clock high time	5.10		0.717	-	
$t_{su(SDA)}$	SDA setup time	1080		1000	-	ns
$t_{h(SDA)}$	SDA hold time	0(3)	451.85	0(4)	457.77(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	Rise time for SDA and SCL	-	381.625	-	389.563	
$t_{f(SDA)}$ $t_{f(SCL)}$	Fall time for SDA and SCL	-	4.33	-	3.79	
$t_{h(STA)}$	Start condition hold time	4.94	-	0.822	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.99	-	0.8124	-	
$t_{su(STO)}$	Stop condition setup time	4.92	-	0.81	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	5.36	-	2.06	-	μs

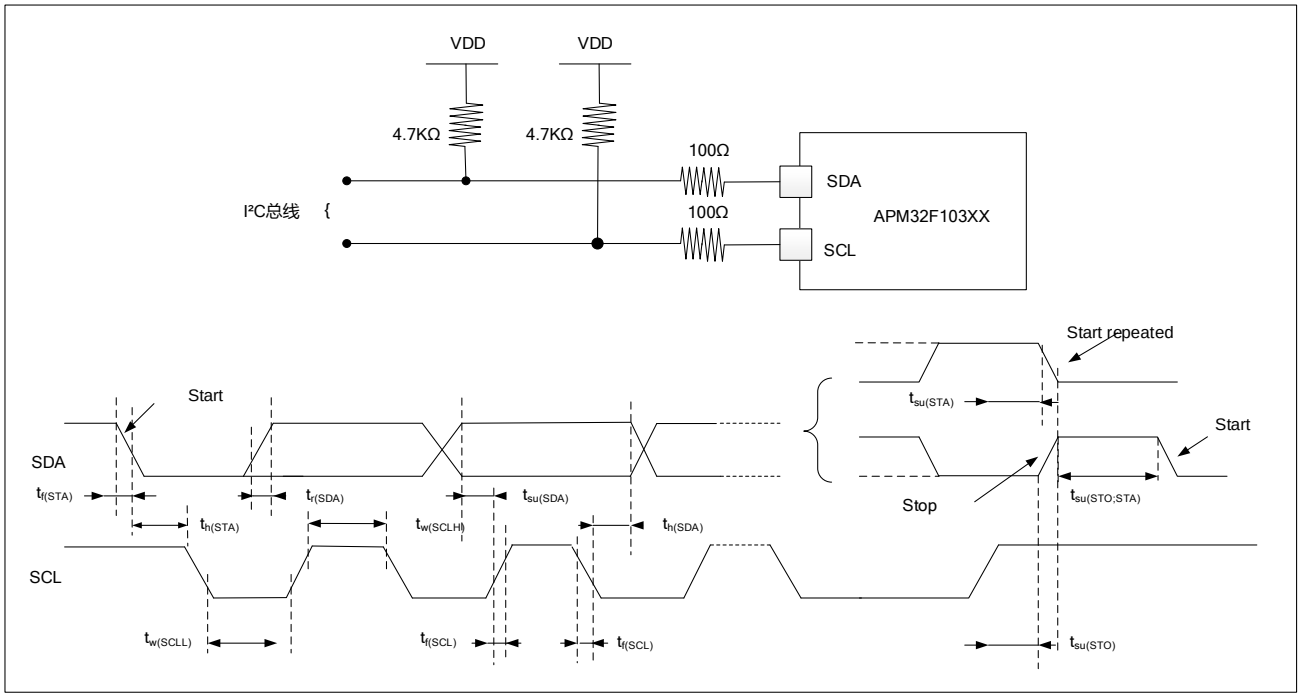
(1) It is guaranteed by design, and is not tested in production.

(2) For the bit to reach the maximum frequency of the standard mode I²C, f_{PCMU1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I²C, f_{PCMU1} must be greater than 4MHz.

(3) If you do not want to stretch the low time of the SCL signal, the maximum hold time of the start condition must be met.

(4) The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.

Figure 12 IC Bus AC Waveform and Measurement Circuit (1)



1. Measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

SPI Interface Characteristics

Table 39 SPI Characteristics (V_{DD} = 3.3V, T_A = 25°C)

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI Clock Frequency	Master mode	-	18	MHz
		Slave Mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall times	Load capacitance: C=30pF	-	3.7	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	109.7	-	ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	85.3	-	ns
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode f_{PCMU} = 36MHz，presc=4	53.9	57.2	ns
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	9.1	-	ns
		Slave mode	19.0	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master Mode	30.0	-	ns
		Slave Mode	21.6	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 20MHz	6.6	10.1	ns
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	6.6	-	ns

Symbol	Parameters	Conditions	Minimum Value	Maximum Value	Unit
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		15.4	ns
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		15.4	ns
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	7.17	-	ns
$t_{h(MO)}$ (2)		Master mode (after enable edge)	7.03	-	

1. The remapped SPI1 characteristics needs further determination.
2. It is derived from calculation and is not tested in production.
3. The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to validate the data.
4. The minimum value represents the minimum time to invalidate the output, and the maximum value represents the maximum time to place the data in Hi-Z.

Figure 13 SPI Timing Diagram - Slave Mode and CPHA=0

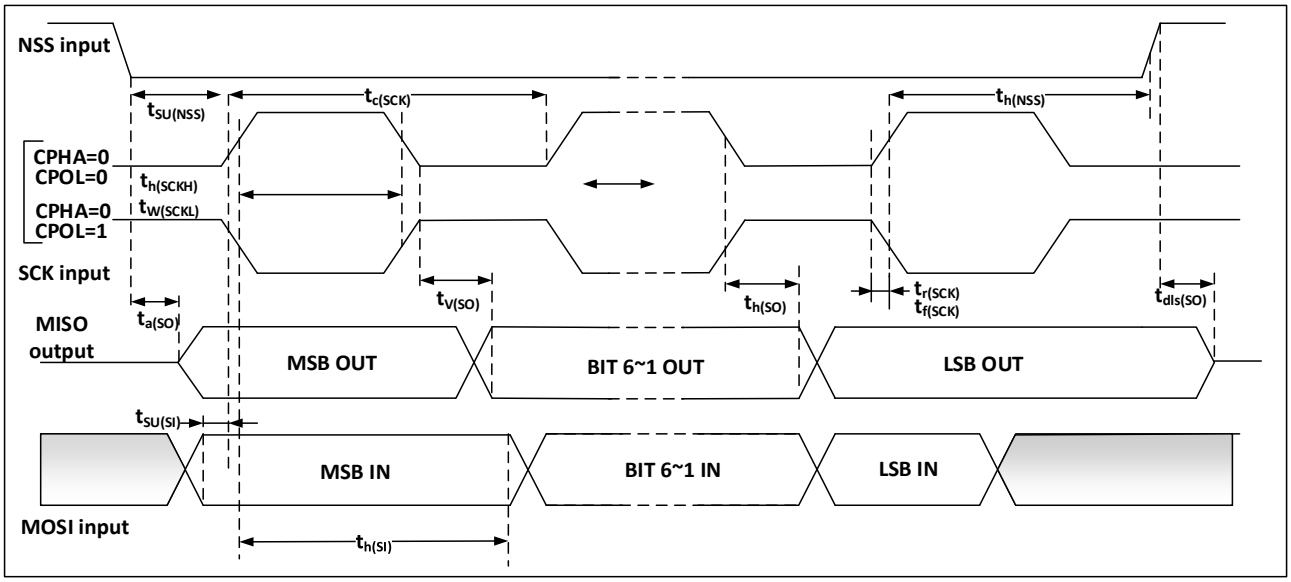
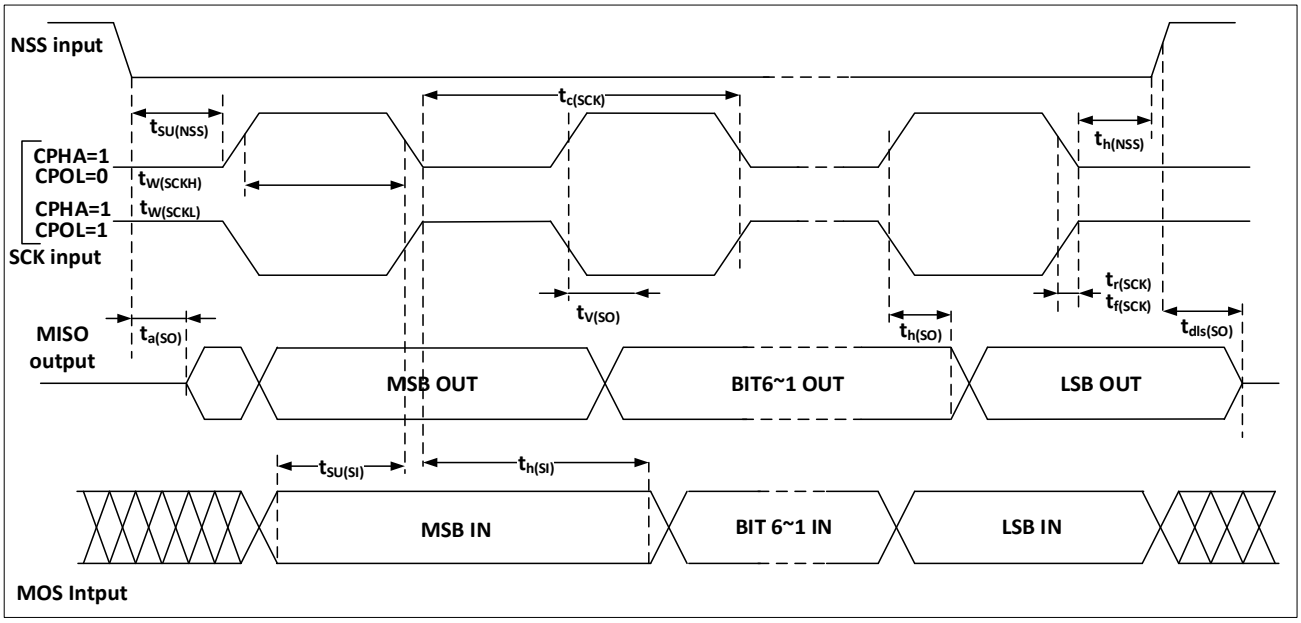
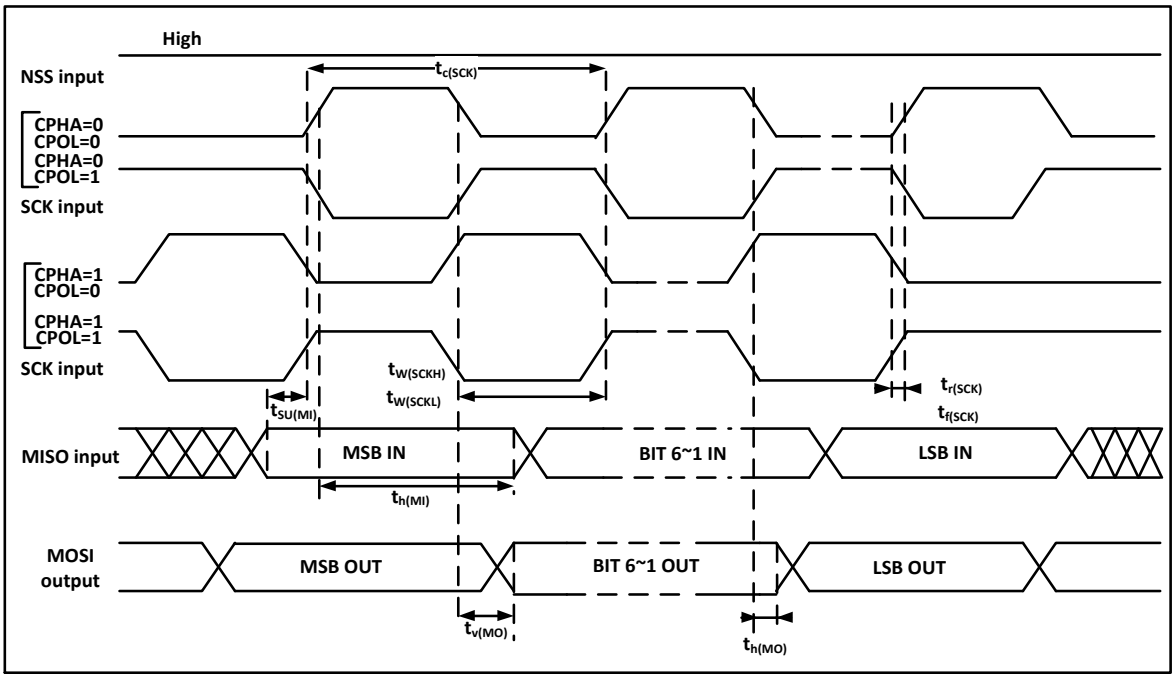


Figure 14 SPI Timing Diagram - Slave Mode and CPHA=1(1)



1. The measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 15 SPI Timing Diagram - Master Mode(3)



1. The measured points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

USBD Interface Characteristics

Figure 16 USBD Timings: Definition of Data Signal Rise and Fall Times

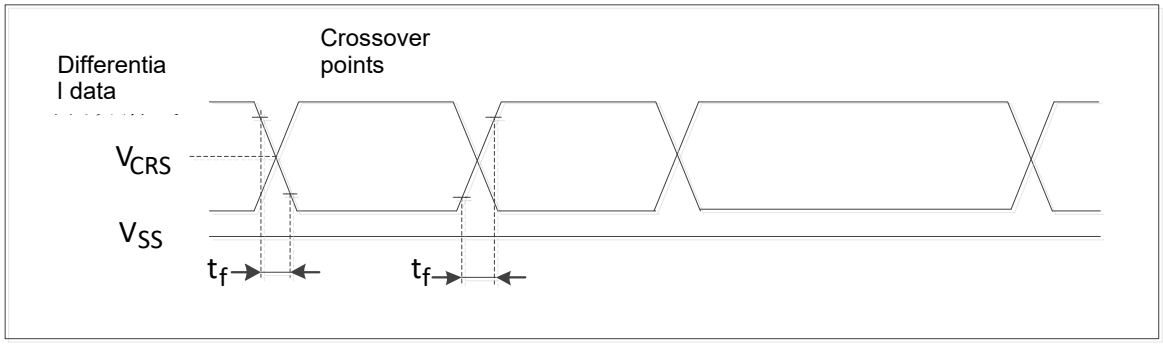


Table 40 USBD Full Speed Electrical Characteristics(V_{DD} = 3.0~3.6V，T_A = 25℃)

Symbol	Parameter	Conditions	Minimum Value(1)	Maximum Value(1)	Unit
Input levels					
V_{DD}	USBD operating voltage (2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I（USBDP，USBDM）	0.2	-	V
V_{CM}(4)	Differential common mode range	Include V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5kΩto 3.6V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 1.5kΩto V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. In order to be compatible with USB2.0 full-speed electrical specification, USBDP (D +) pin must be pulled up with a 1.5 k Ω resistor connected to the voltage from 3.0 V to 3.6 V.
3. The function of APM32F103xDxE is ensured down to 2.7 V but not the electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
4. Guaranteed by comprehensive evaluation and is not tested in production.
5. RL is the load connected on the USBD drivers.

8.3.13 12-bit ADC Characteristics

Table 41 ADC Characteristics (V_{DD} =2.4-3.6V, T_A =-40~105°C)

Symbol	Parameters	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on V_{REF+} input pin	-	-	260	484	μA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{REF+}	V
R_{ADC}(2)	Sampling resistor	-	-	1	-	kΩ
C_{ADC}(2)	Sample and hold capacitor	-	-	2	-	Pf
t_{CAL}	Calibration time	f_{ADC} = 14MHz	5.9			μs
		-	83			$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14MHz	1	-	18	μs
		-	14 to 252(t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

Equation 1: R_{AIN} max formula

$RAIN<Ts/f_{ADC}xC_{ADC}xIn(2^{N+2})-R_{ADC}$

f_{ADC}=14MHz,C_{ADC}=2PF,R_{ADC}=kΩ. For 0.25LSB sampling error accuracy requirements, the relationship between T_S and R_{AIN} is shown in the following table:

Table 42 Maximum R_{AIN} at f_{ADC}=14MHz(1)

T_S (cycle)	t_S (μs)	Maximum R_{AIN} (kΩ)
1.5	0.11	4.5
7.5	0.54	26.6
13.5	0.96	48.7
28.5	2.04	103.9
41.5	2.96	151.7
55.5	3.96	203.2

Table 43 ADC Accuracy

Symbol	Parameter	Conditions	Typical value	Maximum value(3)	Unit
ET	Total error	f_{PCLK2} = 56MHz, f_{ADC} = 14MHz,R_{AIN} < 10kΩ V_{DDA} = 2.4~3.6V,T_A=-40~105℃ Measurement made after ADC calibration	±2.5	±5.5	LSB
Eo	Offset error		±2.1	±3.5	
EG	Gain error		±2.0	±4	
ED	Differential linearity error		±1.5	±2.5	
EL	Integral linearity error		±1.8	±3	

(1) ADC DC accuracy values are measured after internal calibration.

(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

(3) Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.

(4) Guaranteed by comprehensive evaluation and is not tested in production.

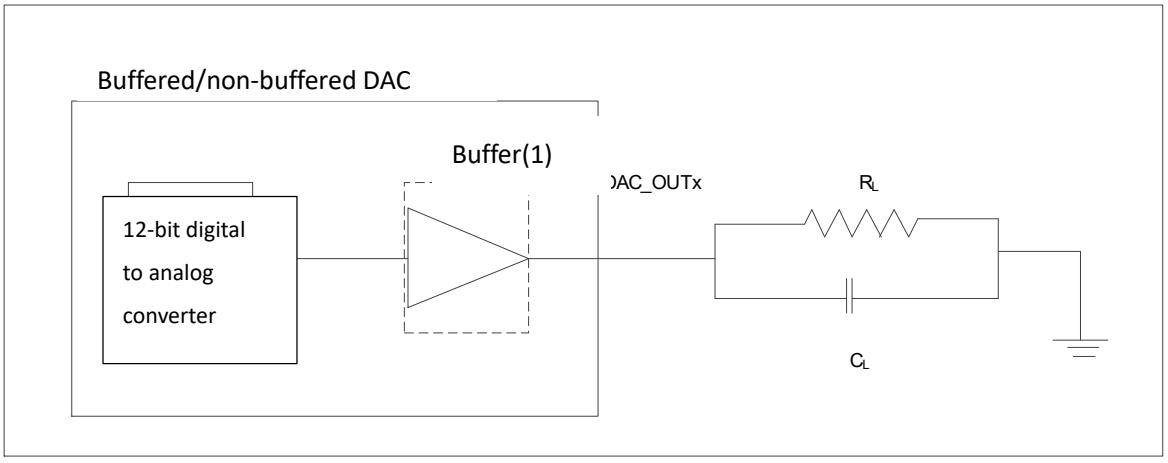
8.3.14 DAC electrical specifications

Figure 44 DAC Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+}must always be below VDDA	2.4	-	3.6	V
V_{SSA}	Ground	-	0	-	0	V
R_{LOAD}	Resistive load with buffer ON	-	5	-		kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).	-	-	50	pF
DAC_OUT min	Lower DAC_OUT voltage with buffer	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at VREF+ = 3.6 V and (0x155) and (0xEAB) at VREF+= 2.4 V	0.186	0.194	0.203	V
DAC_OUT max	Higher output voltage with buffer		-	-	V_{REF+}-0.2	V
DAC_OUT min	Lower DAC_OUT voltage	It gives the maximum output	0.308	-	272.36	mV

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
	with buffer	excursion of the DAC.				
DAC_OUT max	Higher DAC_OUT voltage with buffer		2.381	-	2.398	mV
DNL	Differential non linearity Difference between two consecutive code-1LSB)	DAC in 12-bit configuration	-2.38	-	1.72	LSB
I_{NL}	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	DAC in 12-bit configuration	-6.58	-	6.38	LSB
Offset	Offset error (difference between measured value at Code (0x800) and the ideal value = VREF+/2)	Given for the DAC in 12-bit at VREF+ = 3.6	-6.60	-	9.13	LSB
Gain error	Gain error	DAC in 12-bit configuration	-0.58	-	0.23	%

Figure 17 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

8.3.15 Temperature Sensor Characteristics

Table 45 Temperature Sensor Characteristics

Symbol	Parameters	Minimum Value	Typical Value	Maximum Value	Unit
Avg_Slope(1)	Average slope (V_{DD} = 3.3V, T_A = -40~105°C)	4.1	4.2	4.5	mV/ºC

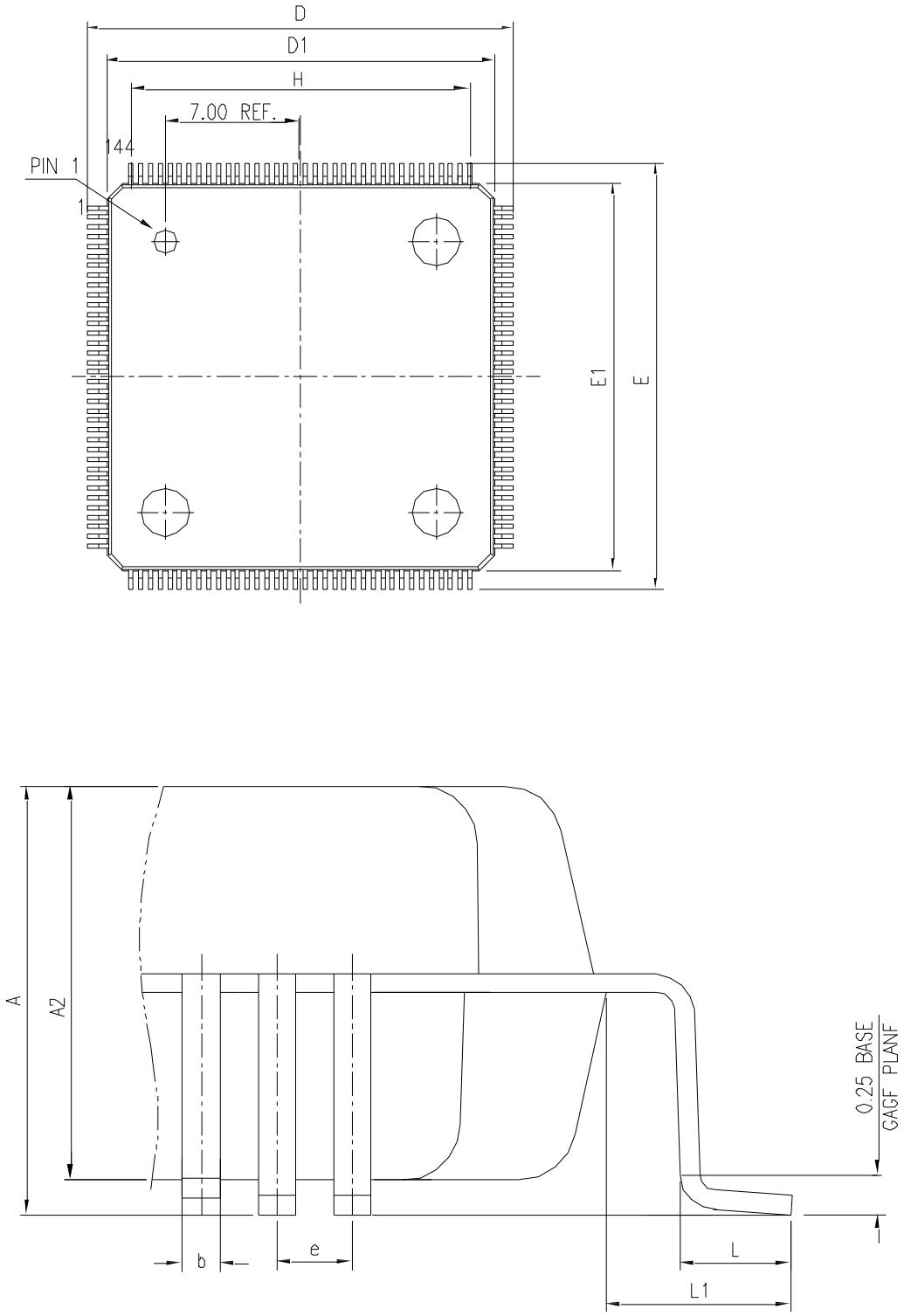
V_{25}	Voltage at 25ºC (V_{DD} =2.4-3.6V)	1.32	1.41	1.5	V
t_{START}(2)	Setup time	4	-	10	μs
T_{S_temp}(2) (3)	ADC sampling time when reading the temperature	-	-	17.1	μs

1. It is guaranteed by characteristics analysis, and is not tested in production.
2. It is guaranteed by design, and is not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.

9 Packaging Information

9.1 LQFP144 Package Diagram

Figure 18 LQFP144 Package Diagram



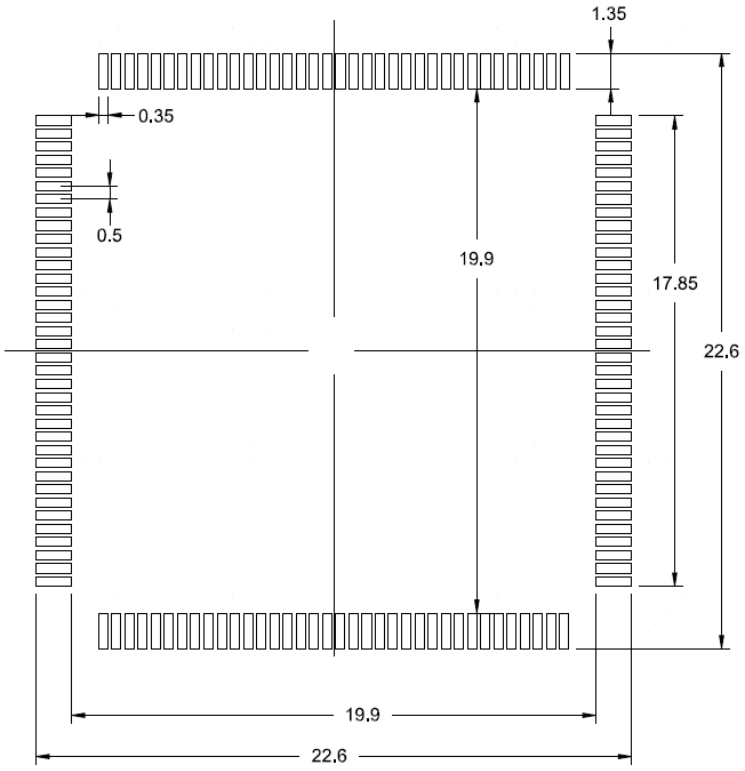
1. Drawing is not to scale.
2. All pins should be soldered to the PCB.

Table 46 LQFP144 Package Data

DIMENSION LIST (FOOTPRINT: 2.00)			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	22.000±0.200	LEAD TIP TO TIP
4	D1	20.000±0.100	PKG LENGTH
5	E	22.000±0.200	LEAD TIP TO TIP
6	E1	20.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF)	(17.50)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

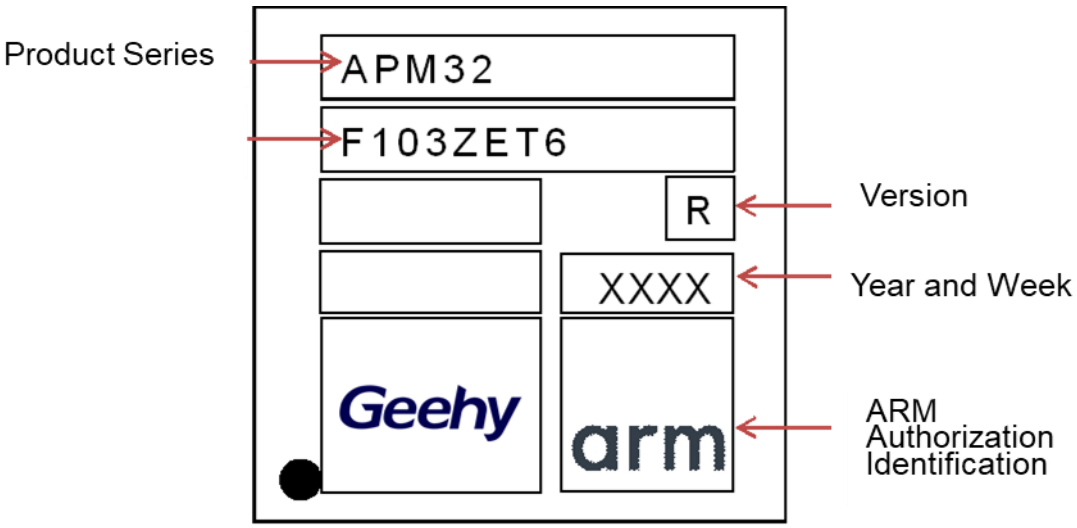
1.dimensions in millimeters.

Figure 19 LQFP144-144 pins, 20 x 20mm recommended welding Layout



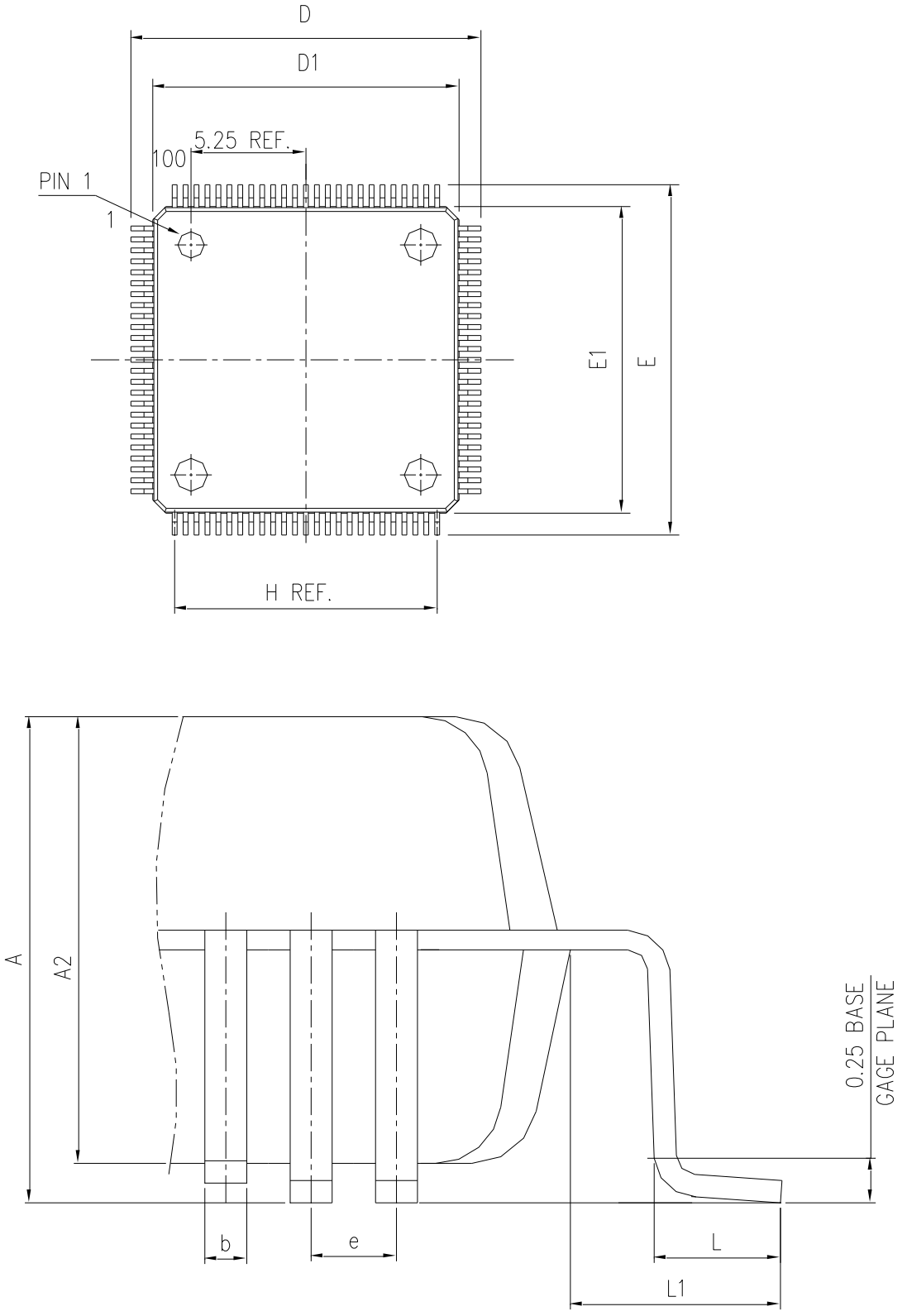
1.dimensions in millimeters.

Figure 20 LQFP144-144 pin, 20 x20 mm package identification diagram



9.2 LQFP100 Package Diagram

Figure 21 LQFP100 Package Diagram



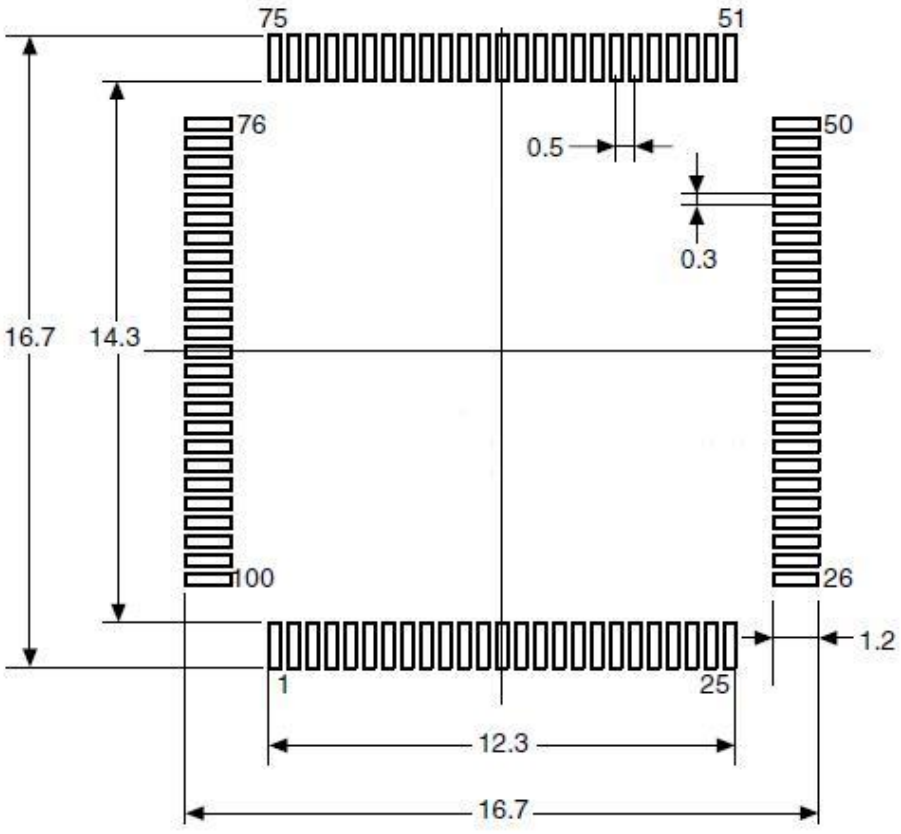
1. Drawing is not to scale.
2. All pins should be soldered to the PCB.

Table 47 LQFP100 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF)	(12.00)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

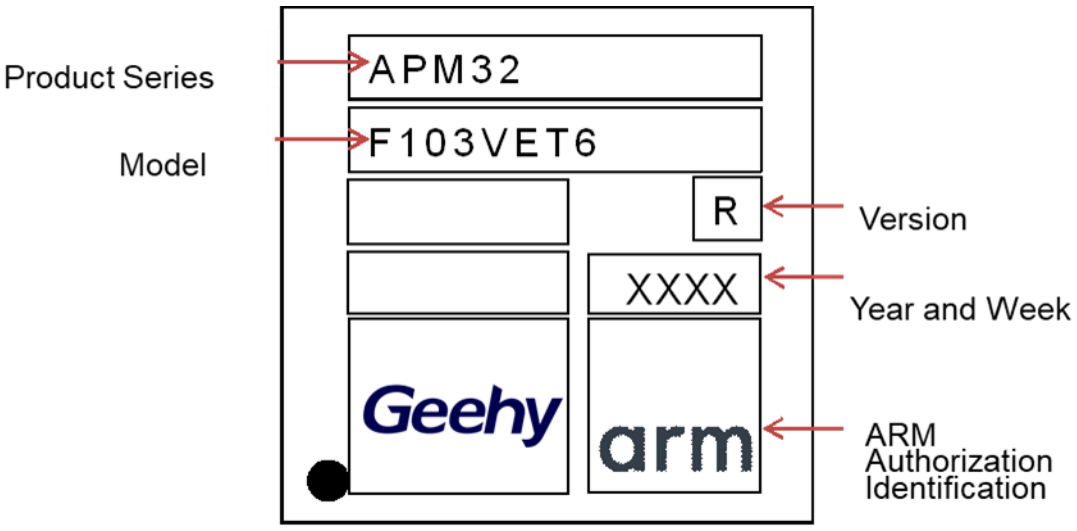
1.Dimensions in millimeters.

Figure 22 LQFP100 - 100 pin, 14 x 14mm recommended welding Layout



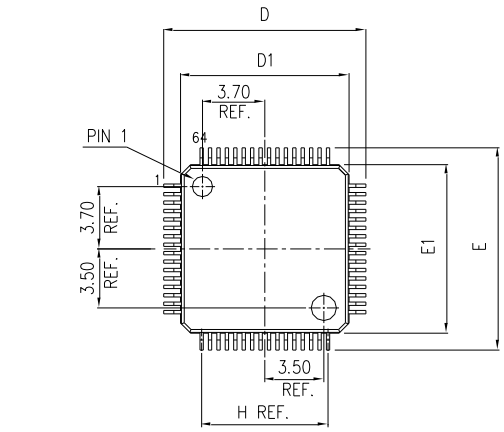
1.Dimensions in millimeters.

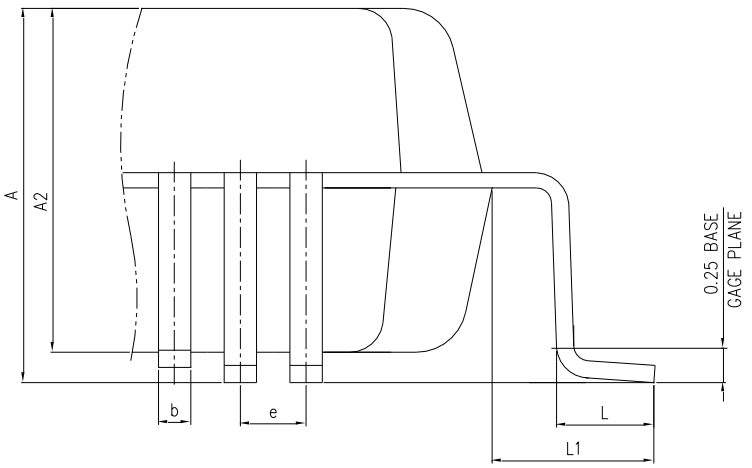
Figure 23 LQFP100 - 100 pin, 14 x 14mm package identification diagram



9.3 LQFP64 Package Diagram

Figure 24 LQFP64 Package Diagram





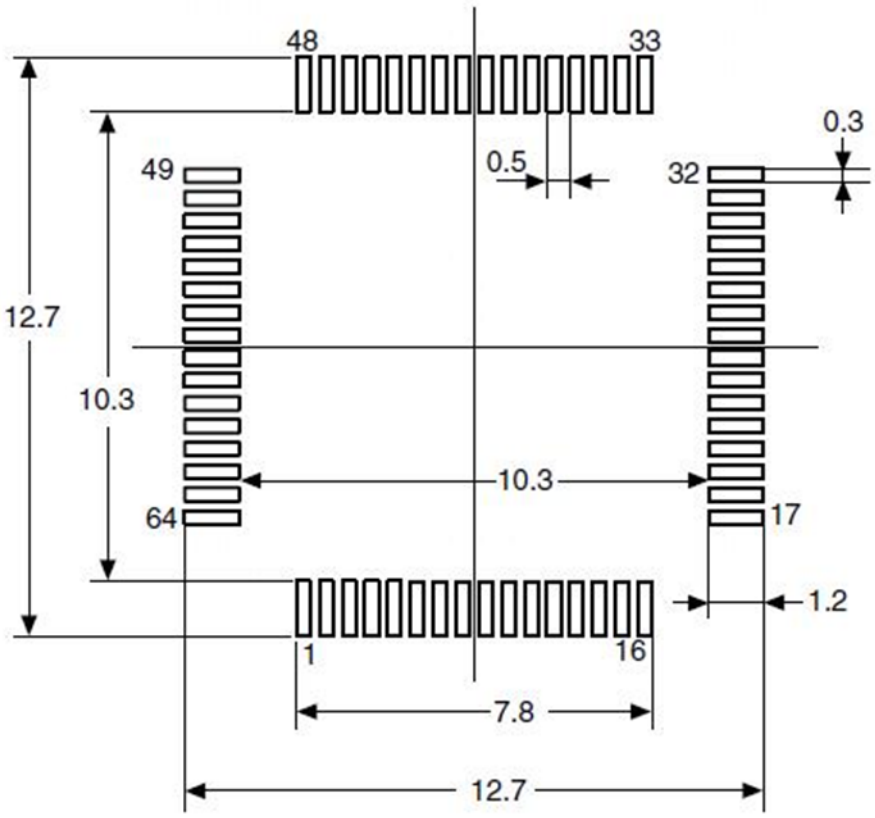
1. Drawing is not to scale.
2. All pins should be soldered to the PCB.

Table 48 LQFP64 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	**SYM**	**DIMENDIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	12.000±0.200	LEAD TIP TO TIP
4	D1	10.000±0.100	PKG LENGTH
5	E	12.000±0.200	LEAD TIP TO TIP
6	E1	10.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H(REF)	(7.500)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

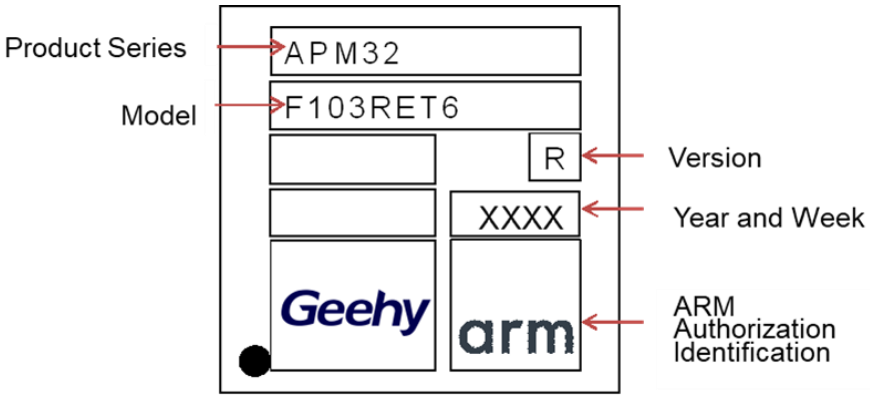
1.Dimensions in millimeters.

Figure 25　LQFP64 - 64 pin, 10 x 10mm recommended welding Layout



1.Dimensions in millimeters.

Figure 26　LQFP64 - 64 pin, 10 x 10mm identification diagram



10 Ordering Information

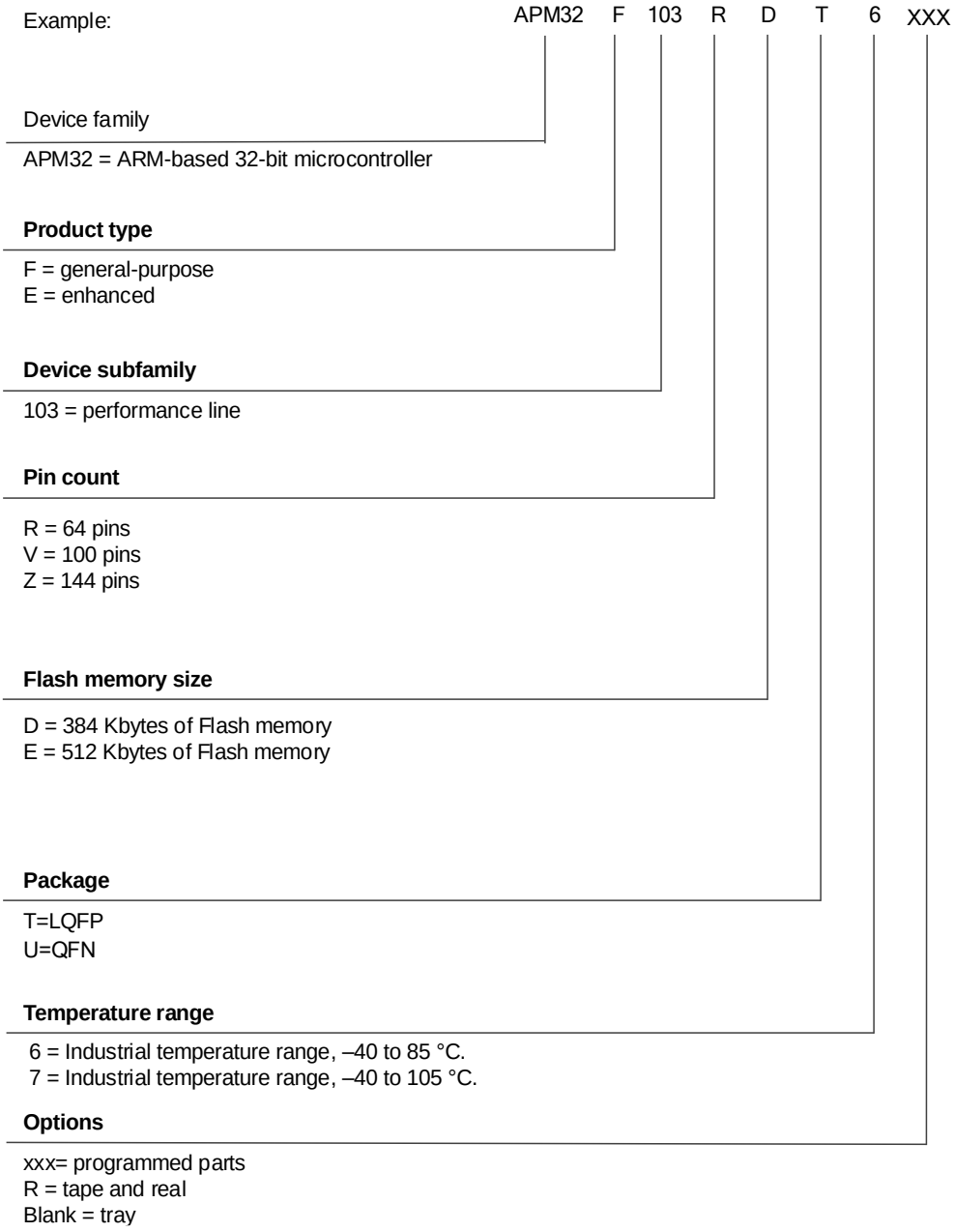


Table 49 Ordering Information Table

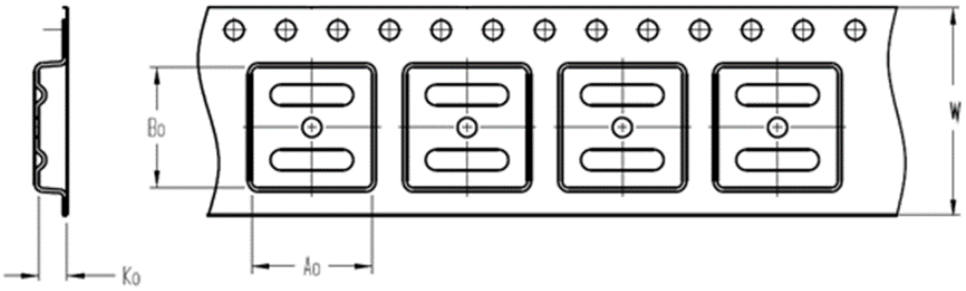
Order No.	FLASH(KB)	RAM(KB)	Package	SPQ	Temperature range
APM32F103RDT6-R	384	64	LQFP64	1000	Industrial level -40℃ ~85℃
APM32F103RDT6	384	64	LQFP64	1600	Industrial level -40℃ ~85℃
APM32F103RET6-R	512	128	LQFP64	1000	Industrial level -40℃

Order No.	FLASH(KB)	RAM(KB)	Package	SPQ	Temperature range
					~85℃
APM32F103RET6	512	128	LQFP64	1600	Industrial level -40℃ ~85℃
APM32F103VDT6	384	64	LQFP100	900	Industrial level -40℃ ~85℃
APM32F103VET6	512	128	LQFP100	900	Industrial level -40℃ ~85℃
APM32F103ZDT6	384	64	LQFP144	600	Industrial level -40℃ ~85℃
APM32F103ZET6	512	128	LQFP144	600	Industrial level -40℃ ~85℃

1. SPQ= Minimum Packaging Quantity

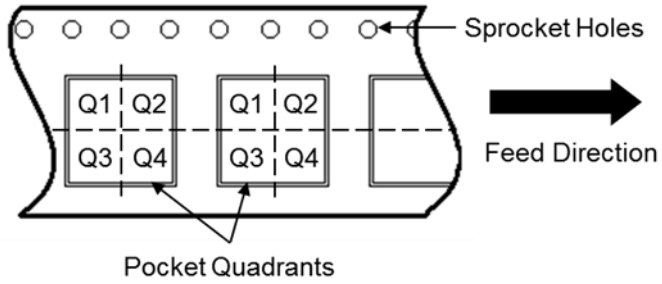
11 Package Information

Figure 27 Specification drawing of ribbon packaging



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions

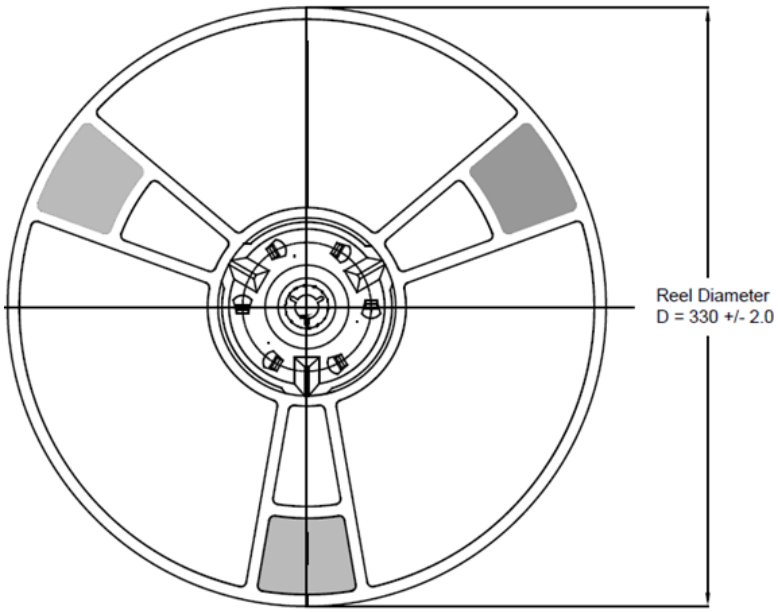
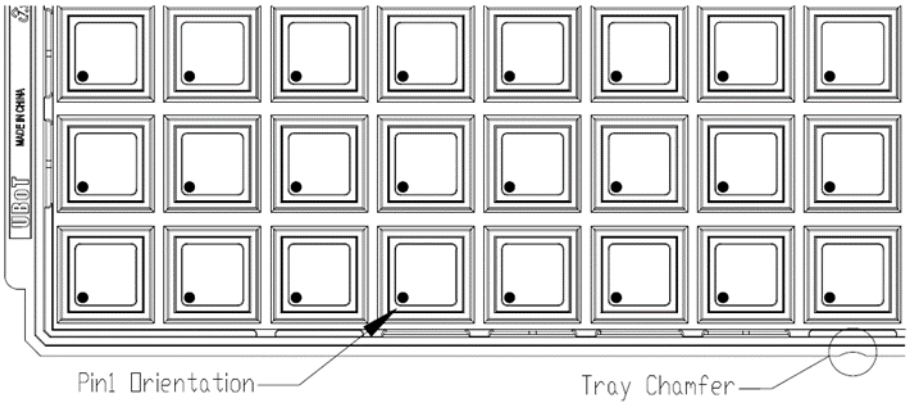


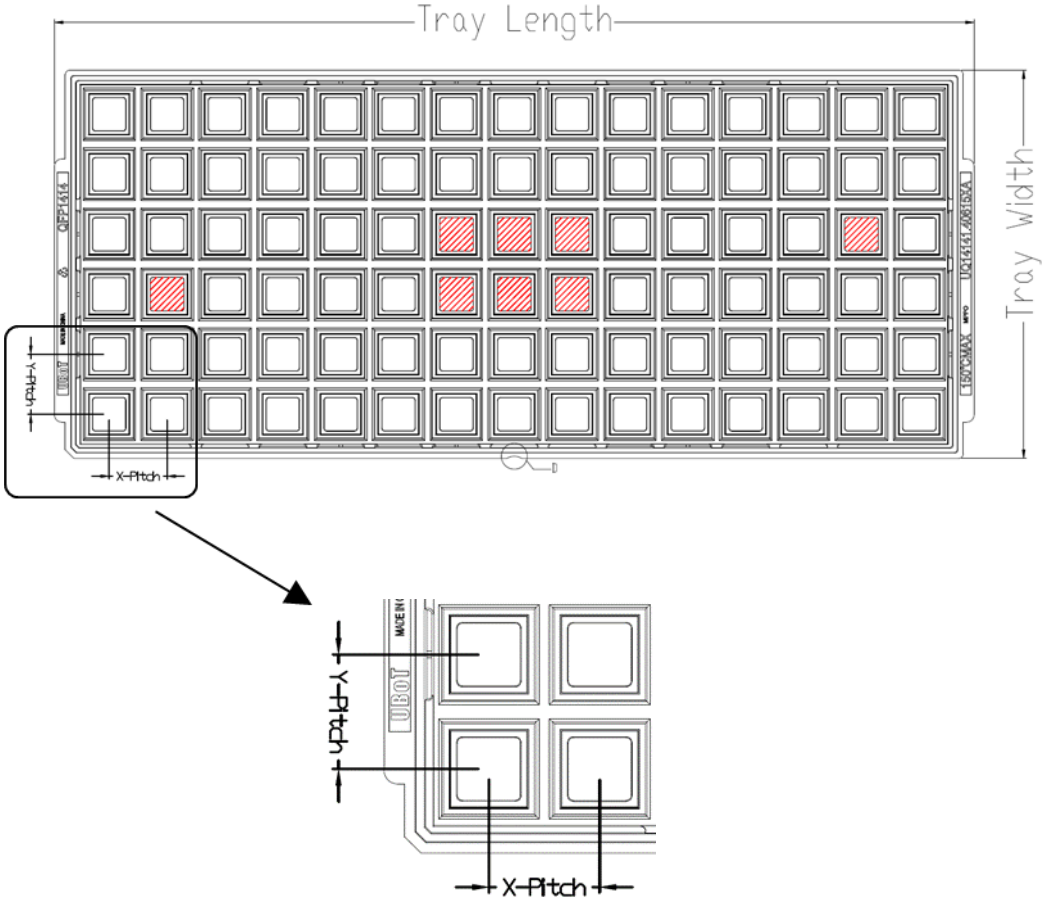
Table 50 Strip Packaging Parameter Specification

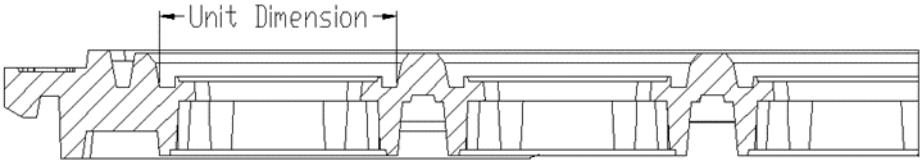
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
APM32F103RET6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
APM32F103RDT6	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

Figure 28 Schematic diagram of pallet packing



Tray Dimensions





All photos are for reference only, appearance is subject to the product.

Table 51 Pallet packing parameters specification sheet

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
APM32F103ZET6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32F103ZDT6	LQFP	144	600	22.06	22.06	25.4	25.2	322.6	135.9
APM32E103VET6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103VET7	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32E103VDT6	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
APM32F103RET6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
APM32F103RDT6	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9

12 Commonly Used Function Module Denomination

Table 52 Commonly Used Function Module Denomination

Commonly Used Function Module Denomination	
Module function	**Abbreviation**
Reset management unit	RMU
Clock management unit	CMU
Reset and Clock management unit	RCM
External Interrupt	EINT
General Purpose IO	GPIO
Alternate Function IO	AFIO
Wakeup controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC Controller	CRC
Power management unit	PMU
The banked register	BAKPR
DMA Controller	DMA
analog-digital converter	ADC
digital-analog converter	DAC
Real-time clock	RTC
External storage controller	EMMC
SDIO Interface	SDIO
USBD Device Controller	USBD
Controller Local Area Network	CAN
USBD OTG	OTG
Ethernet	ETH
I2CcInterface	I2C
Serial Peripheral Interface	SPI
Universal Asynchronous Receiver / Transmitter	UART
Universal Asynchronous/Synchronous Receiver / Transmitter	USART
Flash memory interface control unit	FMC

13 Reversion History

Table 53 Document Reversion History

Date	Version	Changes
2020.02.xx	1.0.0	Initial release
2020.03.05	1.0.1	Note that only 144pin supports SDRAM
2020.03.27	1.1.0	Correct PF11 pin, PF12 pin
2020.5.28	1.2.0	Correct clerical errors in pin and EMC test reference standards
2020.6.22	1.3.0	Whole product characteristics, system block diagram, clock tree, storage map, power supply scheme
2020.7.6	1.3.1	Modify the cover format, modify the SPI feature comment (1)
2020.9.10	1.4	(1) Modify the electrical characteristic data (2) Modify "order code" in "order information list", add "minimum package number", "Flash capacity description", and modify the naming rules of "order information" (3) Modify the function description information in GPIO and add DMC related IO description (4) Adjust the chapter structure (5) Supplement the description of algorithms supported in the section "FPU"
2021.1.20	1.4	(1) Delete the content of APM32F103XC as required (2) Modify APM32F103xCxDxE-APM32F103xDxE,HXT-HSECLK,LXT-LSECLK,HIRC-HSICLK,LIRC-LSICLK,USB-USBD
2021.4.23	1.5	(1) Add APM32F103VET7 model to the packaging information (2) Modify the packaging logo, front cover, back cover and header
2021.8.25	1.6	(1) Modify the table 32 VESD (CDM) as the electrostatic discharge voltage (charging equipment model) (2) Modify the product features in the profile number 1 (originally to 2) (3) Add USBD2 and profile for the common pin, cannot be used at the same time. (4) Modify the NVIC may block channel number is 65 (5) Modifying the clock tree