NS18B20: 1-Wire Digital Thermometer

Datasheet 1.0

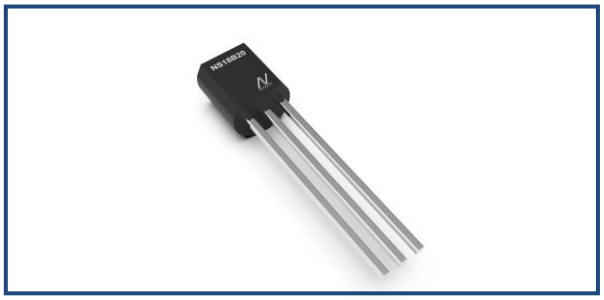
DESCRIPTION

NS18B20 is a high precision 1-wire bus system temperature measurement chip. The temperature range of the temperature sensor is -55 °C to +125 °C. The digital conversion accuracy and temperature measurement speed can be set through the configuration register according to user needs. NS18B20 has a built-in 5byte non-volatile storage unit for users to use. 3byte is used for high and low temperature alarms and configuration accuracy. In addition, 2byte is used to save user-defined information. The nonvolatile storage write cycle takes 10ms. The maximum error of the device is ±1°C over the full temperature range. NS18B20 has two working modes: parasitic power supply and external power supply, in which the parasitic power supply can be powered through the data line without external power supply.

Each NS18B20 has a unique 64-bit serial number. Using a single bus interface allows multiple devices to hang on the same bus. Therefore, this feature can use a processor to control multiple NS18B20 sensors. NS18B20 is widely used in distributed temperature environment monitoring, temperature control and other systems.

FEATURES

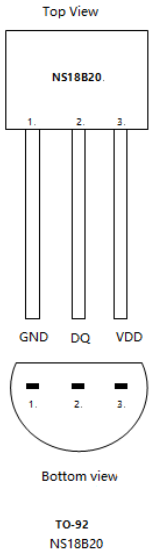
- Unique 1-Wire interface requires only one port pin for communication
- Each Device has a Unique 64-Bit Serial Code Stored in an On-Board ROM
- Measures Temperatures from -55°C to +125°C (-67°F to +257°F)
- Maintain high accuracy in the full temperature range
  - ±0.5°C accuracy from -10°C to +85°C
  - ±1°C accuracy from -55°C to -125°C
- Converts 12-bit temperature to digital word in 50 ms
- No extra pull-up required for temperature conversion
- Requires no external components
- Power supply range is 2.7V to 5.5V
- Thermometer resolution is programmable from 9 to 12 bits
- User-definable, nonvolatile temperature alarm settings
- Available in TO-92 Package



Applications

- Process monitoring and control system
- Industrial Internet of Things
- White goods
- Temperature monitoring

Pin Configuration and Functions



PIN	NAME	FUNCTION
1	GND	Ground
2	DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode.
3	VDD	Optional VDD. VDD must be grounded for operation in parasite power mode.

INDEX

1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

PARAMETER	Symbol	MIN	TYP	MAX	UNIT	NOTES
Supply voltage	VDD	-0.3		5.5	V	25℃
Voltage Range on Any Pin Relative to Ground		-0.3		VDD+0.3	V	25℃
Operating temperature	$TB_{operation}$	-55		125	℃	
Storage temperature		-55		125	℃	
Solder temperature	Refer to IPC / JEDEC J-STD-020 specification					

Note: These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

1.2 DC ELECTRICAL CHARACTERISTICS

-55℃ to +125℃；VDD=2.7V to 5.5V

PARAMETER	Symbol	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDD	Local Power	2.7		5.5	V	1
Pullup Supply Voltage	V_{PU}		2.7		5.5	V	1.2
Thermometer Error	T_{err}	-10℃ to 85℃			0.5	℃	
		-55℃ to 125℃			1		
Input Logic-Low	V_{IL}		-0.3		0.75	V	1,3,4
Input Logic-High	V_{IH}	Local Power	0.7*VDD			V	1,
		Parasite Power	0.7*VDD				
Sink Current	I_L	$V_{I/O}$=0.4V	4.0			mA	1
Standby Current	IDDS			1.5		uA	5,6
Active Current	IDD	V_{DD}=3.3V		26		uA	7
DQ Input Current	IDQ			5		μA	8
Drift				To be determined		℃	9

NOTES:

All voltages are referenced to ground.

The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the NS18B20, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: V_{PU}-ACTUAL = V_{PU_IDEAL} + VTRANSISTOR.

Logic-low voltages are specified at a sink current of 4mA.

To guarantee a presence pulse under low voltage parasite power conditions, VILMAX may have to be reduced to as low as 0.5V.

Logic-high voltages are specified at a source current of 1mA.

To minimize IDDS, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or VDD – 0.3V ≤ DQ ≤ VDD.

Active current refers to supply current during active temperature conversions or EEPROM writes.

DQ line is high ("high-Z" state).

Drift data is based on a 1000-hour stress test at +125°C with VDD = 5.5V.

1.3 AC ELECTRICAL CHARACTERISTICS—NV MEMORY

-55℃ to +125℃；VDD=2.7V to 5.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
NV Write Cycle Time	t_{WR}		10			ms	Non-volatile storage write cycle
EEPROM Writes		-55°C to +55°C	10000			writes	EEPROM write times
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years	EEPROM data retention

1.4 AC ELECTRICAL CHARACTERISTICS

-55℃ to +125℃；VDD=2.7V to 5.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	t_{CONV}	9-bit resolution			50	ms	1
		10-bit resolution			50		
		11-bit resolution			50		
		12-bit resolution			50		
Time to Strong Pullup On		Start Convert T Command Issued			100	µs	
Write EEPROM strong pull-up time			10			ms	
Time Slot	t_{SLOT}		60		120	µs	1
Recovery Time	t_{REC}		1			µs	1
Write 0 Low Time	t_{LOW0}		60		120	µs	1
Write 1 Low Time	t_{LOW1}		1		15	µs	1
Read Data Valid	t_{RDV}				15	µs	1

Reset Time High	t_{RSTH}		480			µs	1
Reset Time Low	t_{RSTL}		480			µs	1,2
Presence-Detect High	t_{PDHIGH}		15		60	µs	1
Presence-Detect Low	t_{PDLOW}		60		240	µs	1
Capacitance	CIN/OUT				25	pF	

NOTES:

1）See the timing diagrams in Figure 18.

2）Under parasite power, if t_{RSTL} > 960µs, a power-on reset may occur.

2. OVERVIEW

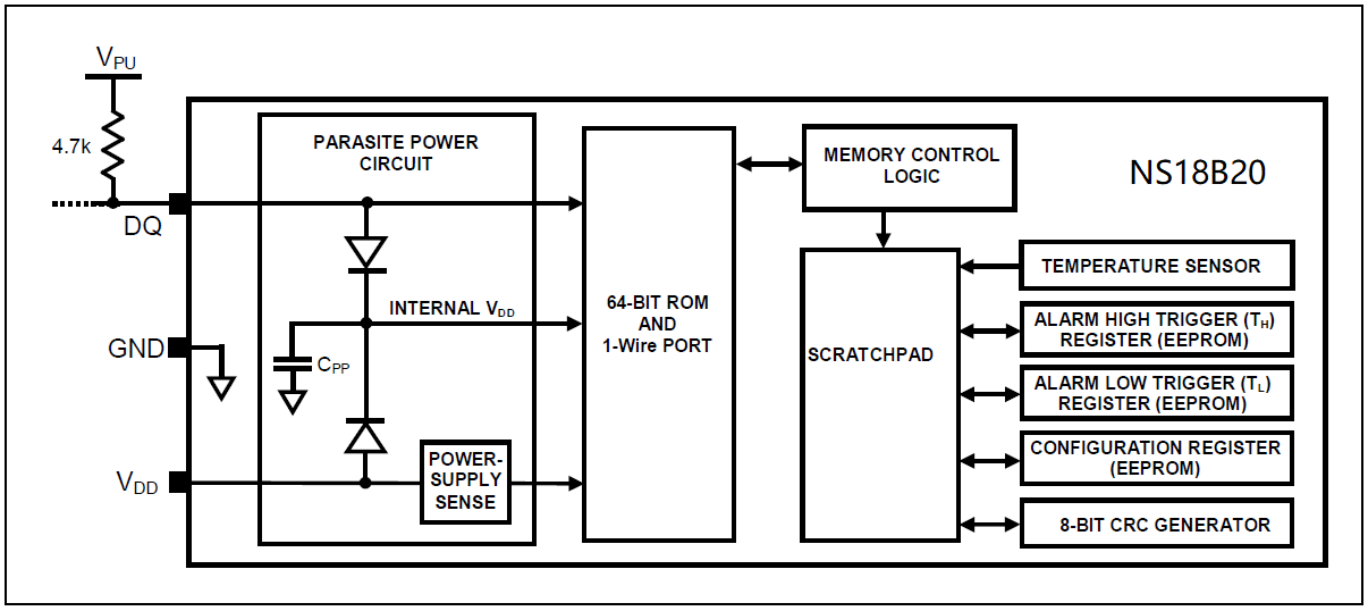


Figure 1. NS18B20 Block Diagram

Figure 1 shows a block diagram of the NS18B20, and pin descriptions are given in the Pin Description table. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (T_H and T_L) and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature-to-digital conversion to 9, 10, 11, or 12 bits. The T_H, T_L, and configuration registers are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The NS18B20 uses Maxim's exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the NS18B20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the 1-Wire Bus System section.

Another feature of the NS18B20 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (C_P), which then

supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as “parasite power.” As an alternative, the NS18B20 may also be powered by an external supply on VDD.

OPERATION - MEASURING TEMPERATURE

The core functionality of the NS18B20 is its direct-to-digital temperature sensor. The resolution of the NS18B20 is configurable (9, 10, 11, or 12 bits), with 12-bit readings the factory default state. This equates to a temperature resolution of 0.5°C, 0.25°C, 0.125°C, or 0.0625°C. The NS18B20 powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the NS18B20 returns to its idle state. If the NS18B20 is powered by an external supply, the master can issue “read time slots” (*see the 1-Wire Bus System section*) after the Convert T command and the NS18B20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the NS18B20 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the *Powering the NS18B20 section.*

The NS18B20 output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two’s complement number in the temperature register (see Figure 2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the NS18B20 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1, and 0 are undefined. Table 1 gives examples of digital output data and the corresponding temperature reading for 12-bit resolution conversions.

	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LS BYTE	0	23	22	21	20	2-1	2-2	2-3	2-4
	ADDR	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
MS BYTE	1	S	S	S	S	S	26	25	24

Figure 2. Temperature Register Format

Table 1. Temperature/Data Relationship

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)				DIGITAL OUTPUT (HEX)
+125	0000	0111	1101	0000	07D0h
+85*	0000	0101	0101	0000	0550h
+25.0625	0000	0001	1001	0001	0191h
+10.125	0000	0000	1010	0010	00A2h
+0.5	0000	0000	0000	1000	0008h
0	0000	0000	0000	0000	0000h
-0.5	1111	1111	1111	1000	FFF8h
-10.125	1111	1111	0101	1110	FF5Eh
-25.0625	1111	1110	0110	1111	FE6Fh

-55	1111 1100 1001 0000	FC90h

2.1 OPERATION—ALARM SIGNALING

After the NS18B20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L registers (see Figure 3). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the Memory section.

Only bits 11 through 4 of the temperature registers are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the NS18B20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

The master device can check the alarm flag status of all NS18B20s on the bus by issuing an Alarm Search [ECh] command. Any NS18B20s with a set alarm flag will respond to the command, so the master can determine exactly which NS18B20s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
High temperature alarm (TH)	2	S	26	25	24	23	22	21	20
	ADDR	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
Low temperature alarm (TL)	3	S	26	25	24	23	22	21	20

Figure 3. TH and TL Register Format

2.2 POWERING THE NS18B20

The NS18B20 can be powered by an external supply on the VDD pin, or it can operate in "parasite power" mode, which allows the NS18B20 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or that are very space constrained. Figure 1 shows the NS18B20's parasite-power control circuitry, which "steals" power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the NS18B20 while the bus is high, and some of the charge is stored on the parasite power capacitor (CPP) to provide power when the bus is low. When the NS18B20 is used in parasite power mode, the VDD pin must be connected to ground.

In parasite power mode, the 1-Wire bus and CPP can provide sufficient current to the NS18B20 for most operations as long as the specified timing and voltage requirements are met (see the DC Electrical Characteristics and AC Electrical Characteristics). However, when the NS18B20 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 2mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by CPP. To assure that the NS18B20 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 4. The 1-Wire bus must be switched to the strong pullup within 10μs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{CONV}) or data transfer (t_{WR} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The NS18B20 can also be powered by the conventional method of connecting an external power supply to the VDD pin, as shown in Figure 5. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time. The use of parasite power is not recommended for temperatures above +100°C since the NS18B20 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the NS18B20 be powered by an external power supply.

In some situation the bus master may not know whether the NS18B20s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read time slot". During the read time slot, parasite powered NS18B20s will pull the bus low, and externally powered NS18B20s will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

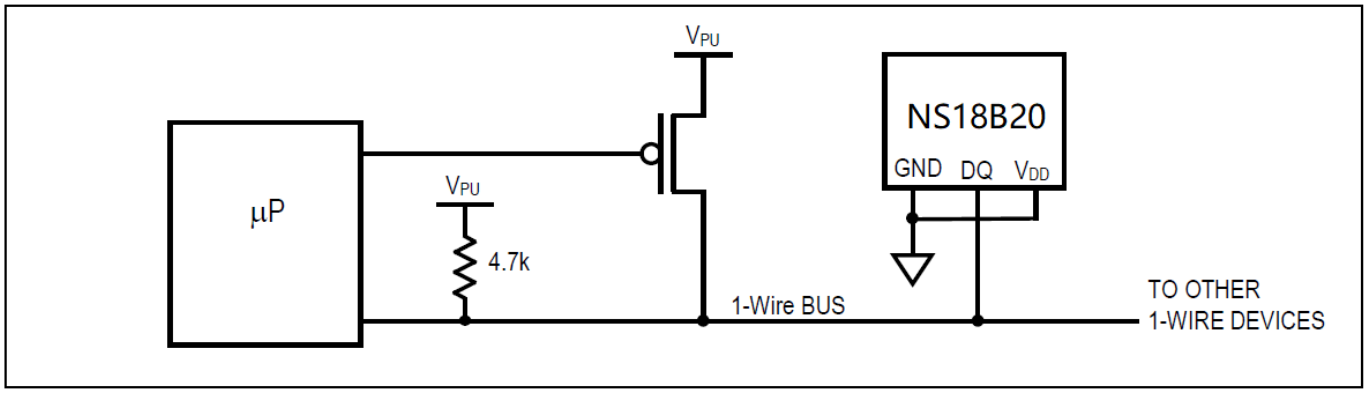


Figure 4. Supplying the Parasite-Powered NS18B20 During Temperature Conversions

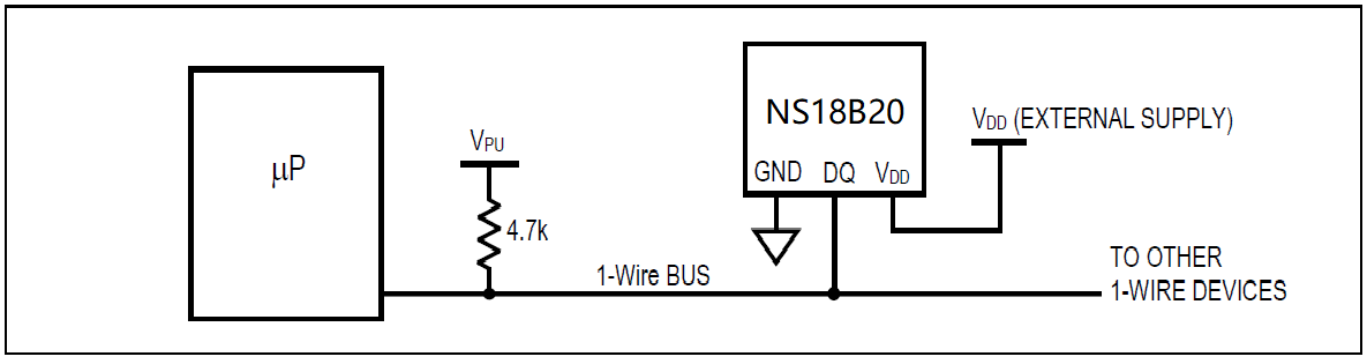


Figure 5. Powering the NS18B20 with an External Supply

2.3 64-BIT LASERED ROM CODE

Each NS18B20 contains a unique 64–bit code (see Figure 6) stored in ROM. The least significant 8 bits of the ROM code contain the NS18B20's 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the *CRC Generation section*. The 64-bit ROM code and associated ROM function control logic allow the NS18B20 to operate as a 1-Wire device using the protocol detailed in the 1-Wire Bus System section.

8-BIT CRC		48-BIT SERIAL NUMBER		8-BIT FAMILY CODE (28h)	
MSB	LSB	MSB	LSB	MSB	LSB

Figure 6. 64-Bit Lasered ROM Code

2.4 MEMORY

The NS18B20's memory is organized as shown in Figure 7. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (T_H and T_L) and configuration register. Note that if the NS18B20 alarm function is not used, the T_H and T_L registers can serve as general-purpose memory. All memory commands are described in detail in the *NS18B20 Function Commands section.*

Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to T_H and T_L registers. Byte 4 contains the configuration register data, which is explained in detail in the Configuration Register section. Bytes 5, 6, and 7 are reserved for internal use by the device and cannot be overwritten.

Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The NS18B20 generates this CRC using the method described in the CRC Generation section.

Scratchpad 2 consists of only 2 bytes and does not have cyclic redundancy check code. Both byte 0 and byte 1 are used to store user register data.

Data is written to bytes 2, 3, and 4 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the NS18B20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H, T_L and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command. Similarly, if user data is to be transferred from the scratchpad to the EEPROM, the host must issue the Copy Custom Scratchpad [28h] command. Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E^2 [B8h] command. The master can issue read time slots following the Recall E^2 command and the NS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

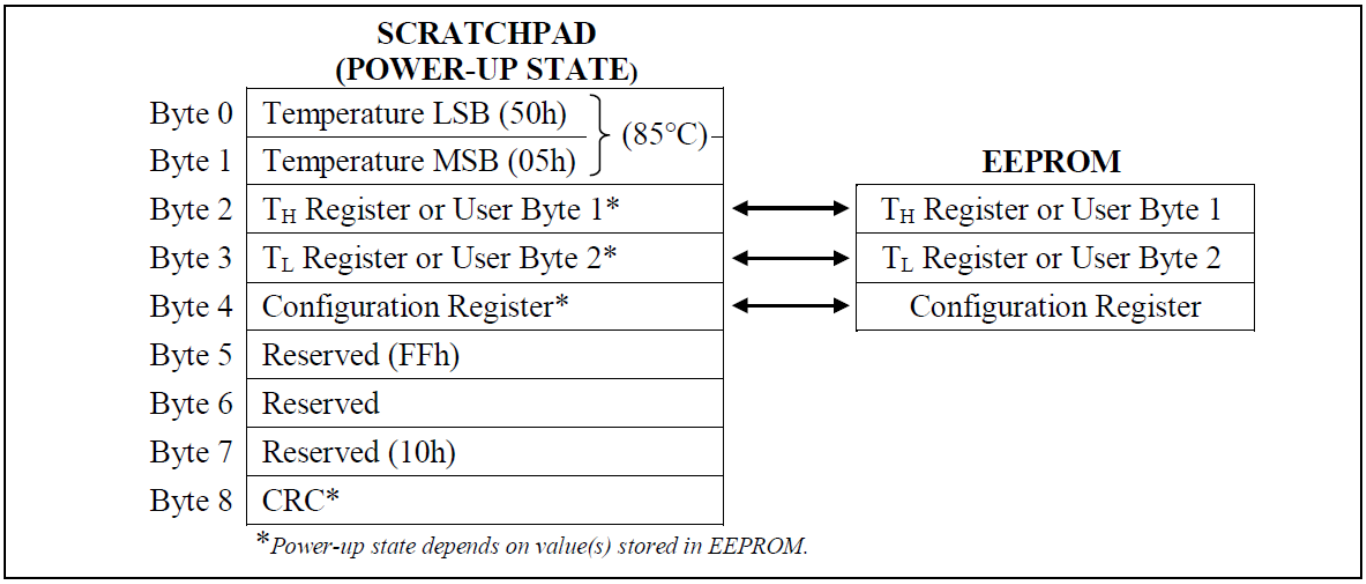


Figure 7. NS18B20 Memory Map

2.5 CONFIGURATION REGISTER

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 8. The user can set the conversion resolution of the NS18B20 using the R0 and R1 bits in this register as shown in Table 2. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that there is a direct tradeoff between resolution and conversion time. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	R1	R0	1	1	1	1	1

Figure 8. Configuration Register

Table 2. Thermometer Resolution Configuration

R1	R0	RESOLUTION (BITS)
0	0	9
0	1	10
1	0	11
1	1	12

2.6 CRC GENERATION

CRC bytes are provided as part of the NS18B20's 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the NS18B20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the NS18B20 that prevents a command sequence from proceeding if the NS18B20 CRC (ROM or scratchpad) does not match the value generated by the bus master.

The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the NS18B20 using the polynomial generator shown in Figure 9. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the NS18B20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s.

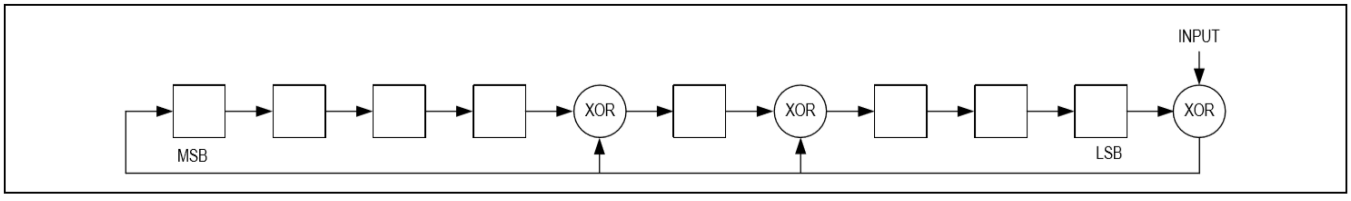


Figure 9. CRC Generator

3. 1-WIRE BUS SYSTEM

The 1-Wire bus system uses a single bus master to control one or more slave devices. The NS18B20 is always a slave. When there is only one slave on the bus, the system is referred to as a “single-drop” system; the system is “multidrop” if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

3.1 HARDWARE CONFIGURATION

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to “release” the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the NS18B20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.

The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480μs, all components on the bus will be reset.

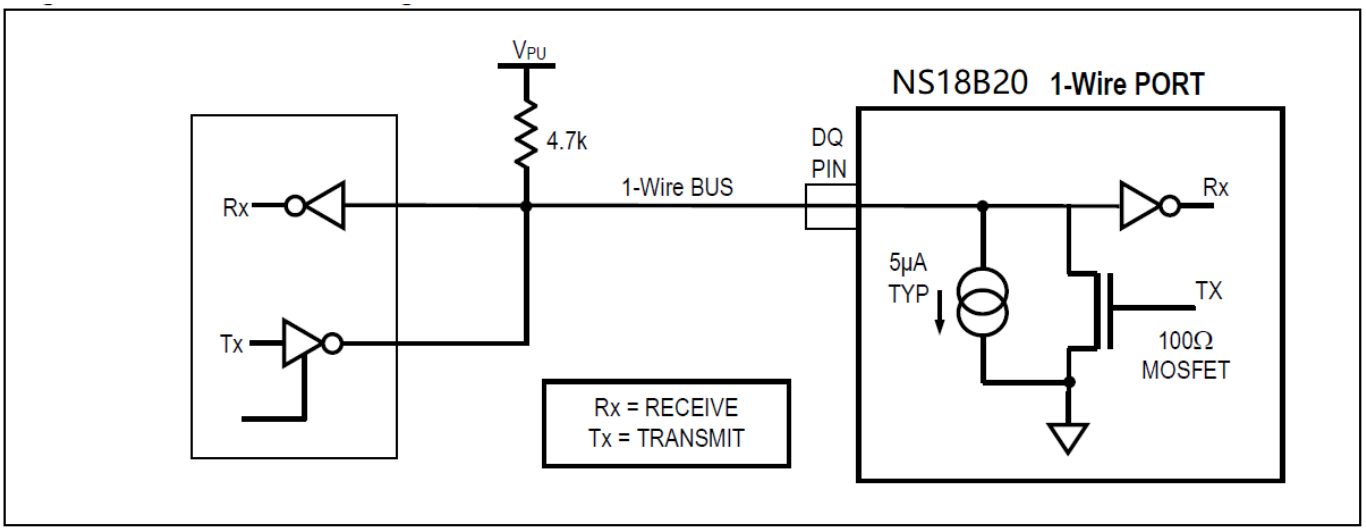


Figure 10. Hardware Configuration

3.2 TRANSACTION SEQUENCE

The transaction sequence for accessing the NS18B20 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. NS18B20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the NS18B20 is accessed, as the NS18B20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

3.2.1 INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the NS18B20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the 1-Wire Signaling section.

3.2.2 ROM COMMANDS

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a NS18B20 function command. A flowchart for operation of the ROM commands is shown in Figure 11.

3.2.3 SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command [33h] can be used in place of the Search ROM process. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

Read ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

Match ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

Skip ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all NS18B20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

Alarm Search [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any NS18B20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. See the Operation—Alarm Signaling section for an explanation of alarm flag operation.

3.2.4 NS18B20 FUNCTION COMMANDS

After the bus master has used a ROM command to address the NS18B20 with which it wishes to communicate, the master can issue one of the NS18B20 function commands. These commands allow the master to write to and read from the NS18B20's scratchpad

memory, initiate temperature conversions and determine the power supply mode. The NS18B20 function commands, which are described below, are summarized in Table 3 and illustrated by the flowchart in Figure 12.

Convert T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the NS18B20 returns to its low-power idle state. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{CONV}) as described in the Powering the NS18B20 section. If the NS18B20 is powered by an external supply, the master can issue read time slots after the Convert T command and the NS18B20 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

Write Scratchpad [4Eh]

This command allows the master to write 3 bytes of data to the NS18B20's scratchpad. The first data byte is written into the T_H register (byte 2 of the scratchpad), the second byte is written into the T_L register (byte 3), and the third byte is written into the configuration register (byte 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

Read Scratchpad [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

Copy Scratchpad [48h]

This command copies the contents of the scratchpad T_H, T_L and configuration registers (bytes 2, 3 and 4) to EEPROM. If the device is being used in parasite power mode, within 10μs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the Powering the NS18B20 section.

Recall E2 [B8h]

This command recalls the alarm trigger values (T_H and T_L) and configuration data from EEPROM and places the data in bytes 2, 3, and 4, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E2 command and the NS18B20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

Write Custom Scratchpad [2Eh]

This command allows the host to write 2 bytes of data into the Scratchpad 2 of the NS18B20 scratchpad. The first byte is written to user register 1 (byte 0 of Scratchpad 2) and the second byte is written to user register 2 (byte 1 of Scratchpad 2). Data transmission starts with the least significant bit. All 2 bytes must be written before the host sends a reset signal, otherwise the data may be damaged.

Read Custom Scratchpad [DEh]

This command allows the host to read the contents of scratchpad 2. The data transfer starts at the lowest bit of byte 0 and continues to traverse to the highest bit of byte 1 to be read. If only part of the data in the scratchpad needs to be read, the host can issue a reset signal at any time to terminate the read operation.

Copy Custom Scratchpad [28h]

This instruction writes 2 bytes of user data in scratchpad 2 to EEPROM. If the slave device is in the parasitic power supply mode, within 10μs after the issuance of this instruction, the master must strongly pull up the single bus and continue the entire copy operation period.

Recall Custom E2 [D8h]

This instruction reloads the user register from the EEPROM and replaces the data corresponding to byte 0 and byte 1 in scratchpad 2. The host can issue a read time slot after the Recall Custom E^2 command, and then the NS18B20 will respond to the current reload status. Sending 0 means that the reload is in progress and sending 1 means that the reload has ended. The reload operation is performed automatically at power-on, so the temporary memory is immediately available after the device is powered on.

Read Power Supply [B4h]

The master device issues this command followed by a read time slot to determine if any NS18B20s on the bus are using parasite power. During the read time slot, parasite powered NS18B20s will pull the bus low, and externally powered NS18B20s will let the bus remain high. See the Powering the NS18B20 section for usage information for this command.

Table 3. NS18B20 Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITYAFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	NS18B20 transmits conversion status to master (not applicable for parasite-powered NS18B20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	NS18B20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to NS18B20.	3
Copy Scratchpad	Copies T_H, T_L, and configuration register data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	NS18B20 transmits recall status to master.	
Read Custom Scratchpad	Read user register contents	DEh	NS18B20 transmits up to 2 bytes to the host	2
Write Custom Scratchpad	Write data to Scratchpad 2 register	2Eh	The host transmits 2 bytes to NS18B20	3
Copy Custom Scratchpad	Copy user register data from scratchpad to EEPROM	28h	None	1
Recall Custom E^2	Reload user register data from EEPROM to scratchpad	D8h	NS18B20 transmits reload status to host	
Read Power Supply	Signals NS18B20 power supply mode to the master.	B4h	NS18B20 transmits supply status to master.	

Note 1: For parasite-powered NS18B20s, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.

Note 2: The master can interrupt the transmission of data at any time by issuing a reset.

Note 3: All three bytes must be written before a reset is issued.

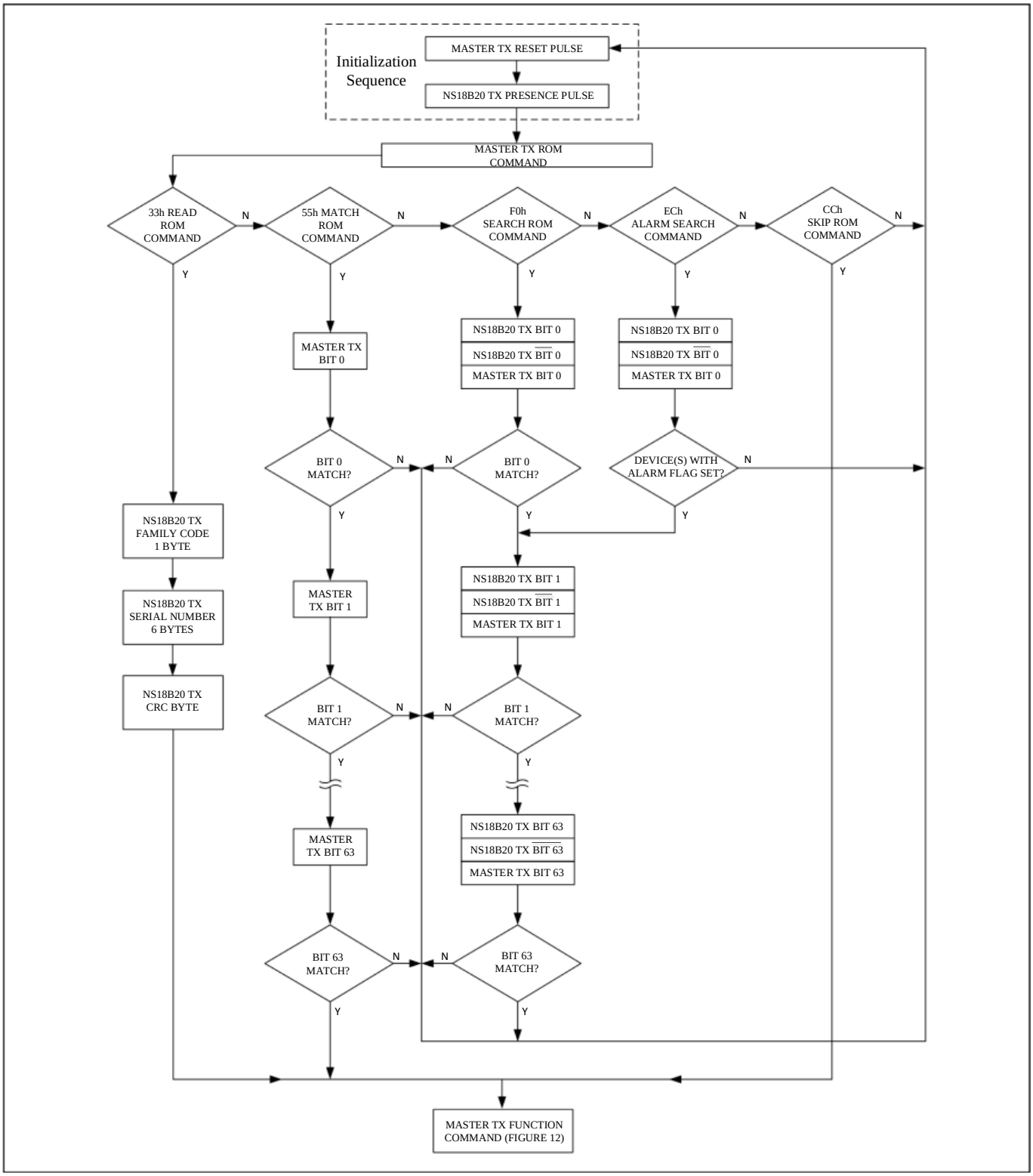


Figure 11. ROM Commands Flowchart

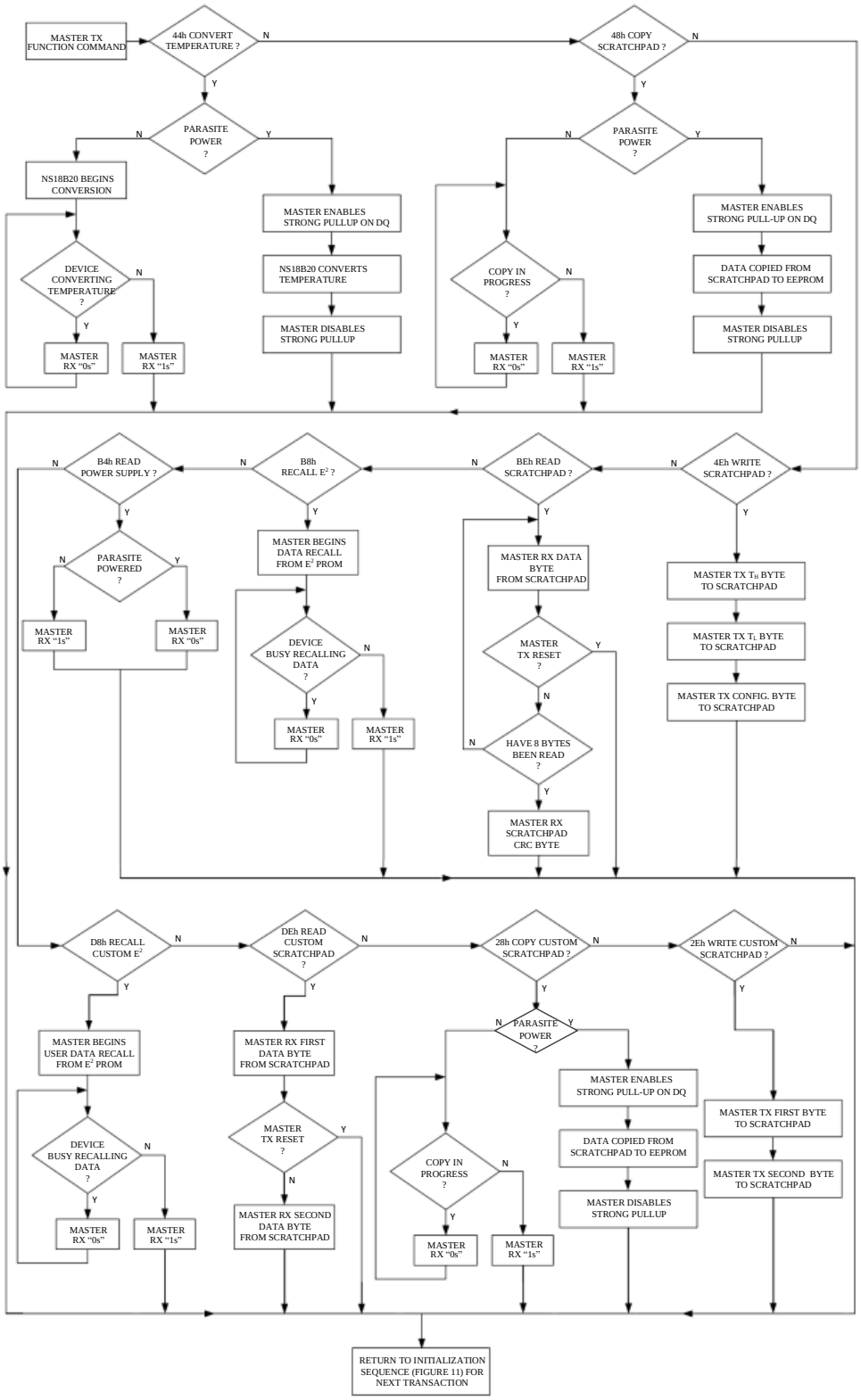


Figure 12. NS18B20 Function Commands Flowchart

3.3 1-WIRE SIGNALING

The NS18B20 uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

INITIALIZATION PROCEDURE—RESET AND PRESENCE PULSES

All communication with the NS18B20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the NS18B20. This is illustrated in Figure 13. When the NS18B20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (TX) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (RX). When the bus is released, the 5kΩ pullup resistor pulls the 1-Wire bus high. When the NS18B20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

READ/WRITE TIME SLOTS

The bus master writes data to the NS18B20 during write time slots and reads data from the NS18B20 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

WRITE TIME SLOTS

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to the NS18B20 and a Write 0 time slot to write a logic 0 to the NS18B20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 14).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5kΩ pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs).

The NS18B20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the NS18B20. If the line is low, a 0 is written to the NS18B20.

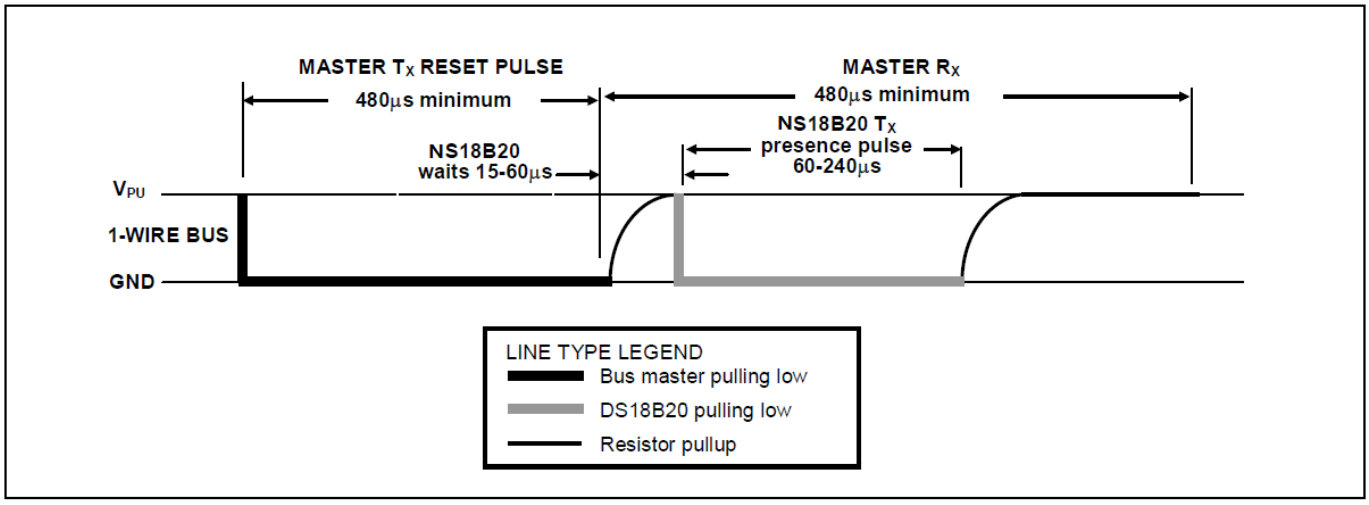


Figure 13. Initialization Timing

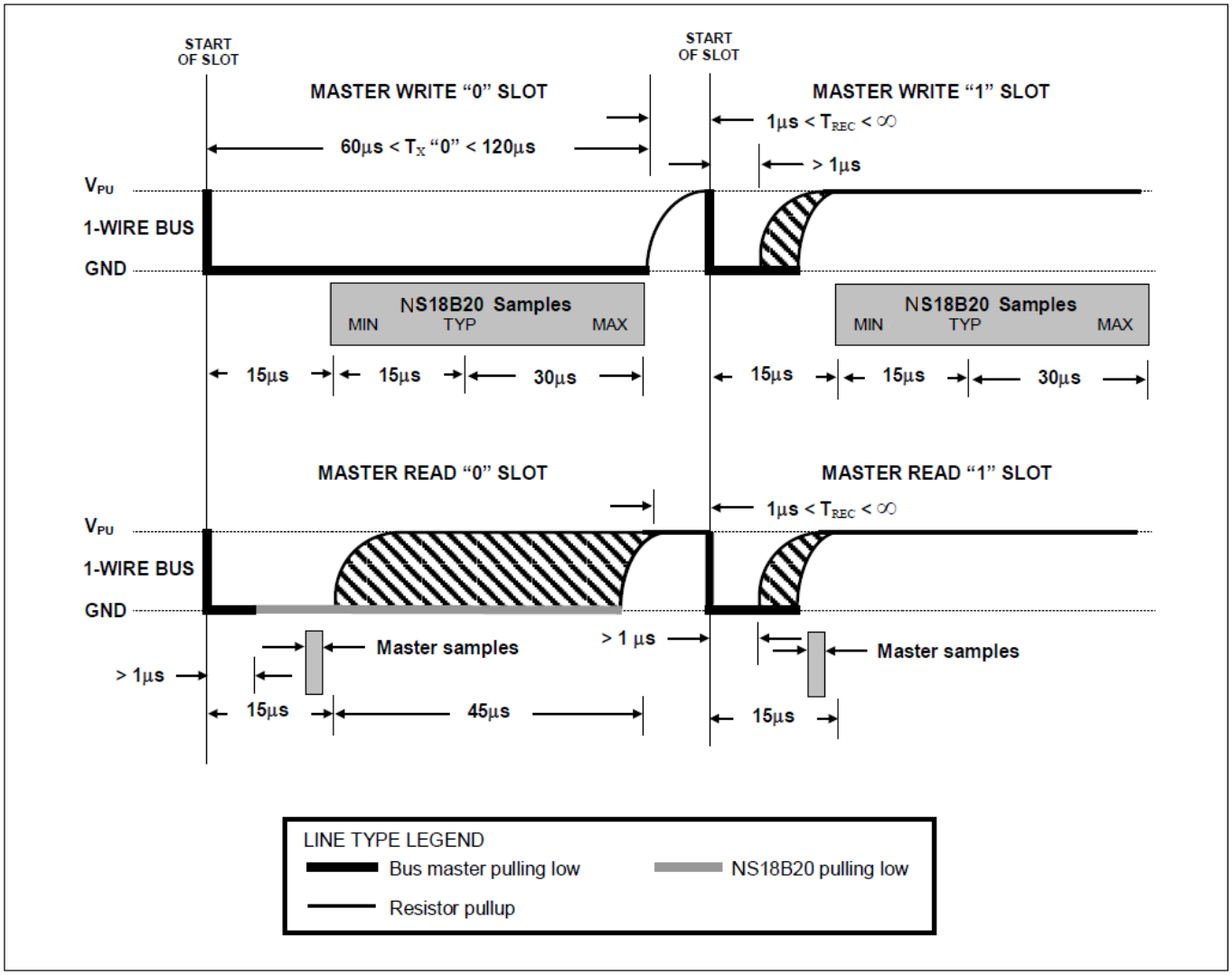


Figure 14. Read/Write Time Slot Timing Diagram

READ TIME SLOTS

The NS18B20 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the NS18B20 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E^2 [B8h]/ Recall Custom E^2 [D8h] commands to find out the status of the operation as explained in the NS18B20 Function Commands section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 14). After the master initiates the read time slot, the NS18B20 will begin transmitting a 1 or 0 on bus. The NS18B20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the NS18B20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output data from the NS18B20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot. Figure 15 illustrates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs for a read time slot. Figure 16 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.

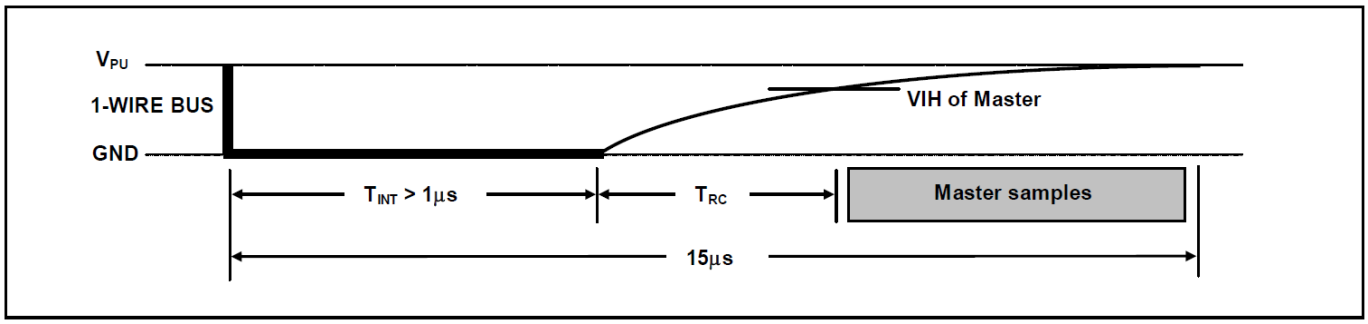


Figure 15. Detailed Master Read 1 Timing

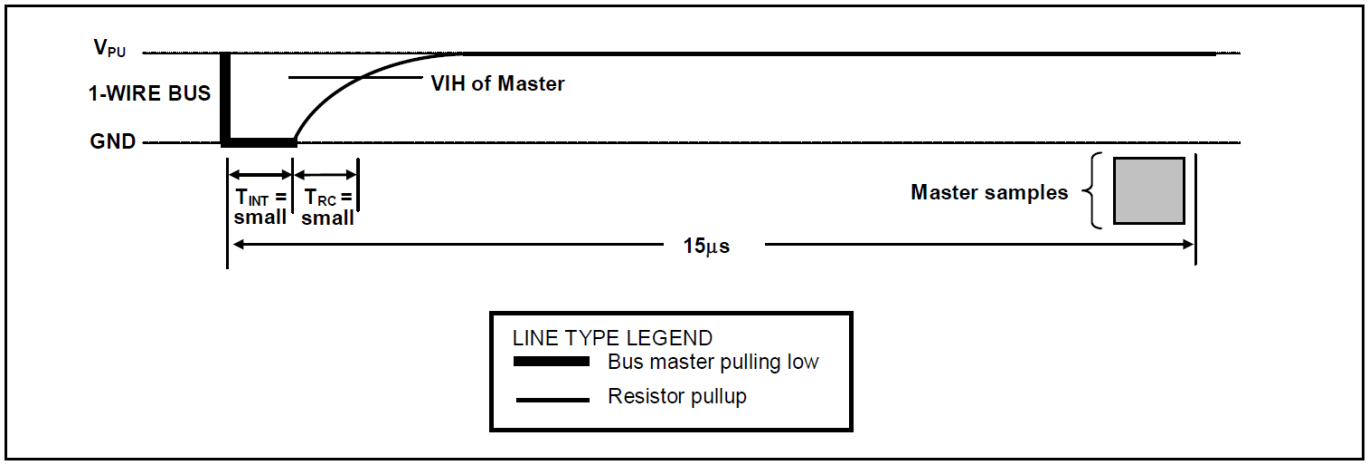
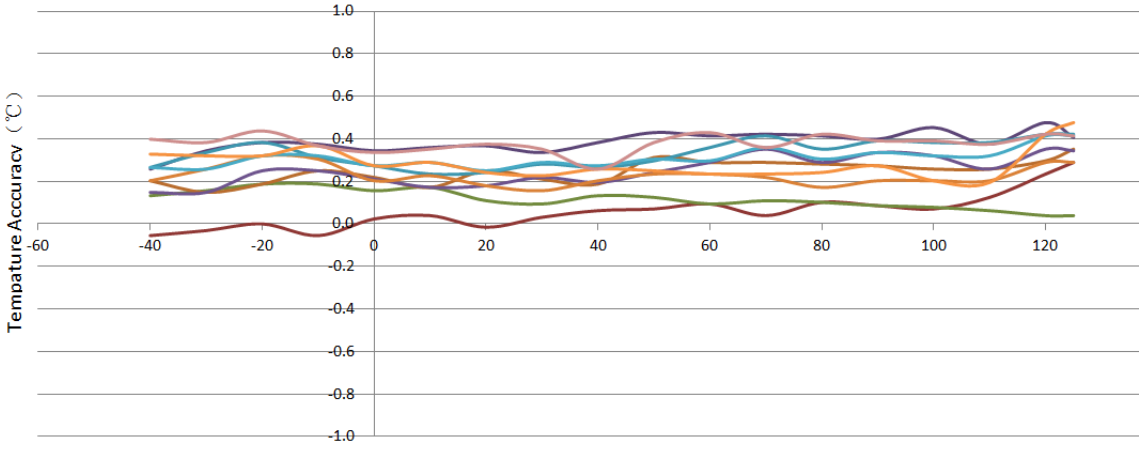


Figure 16. Recommended Master Read 1 Timing

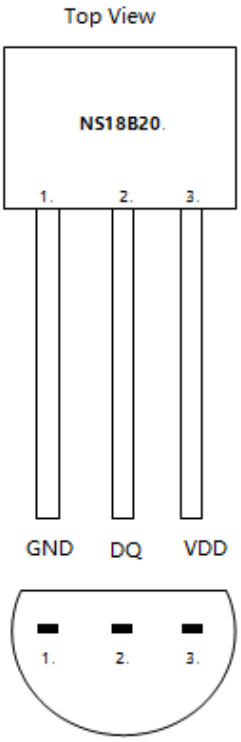
4. Typical Characteristics



Use To-92 package test, VDD voltage is 5V

5. PACKAGE MATERIALS INFORMATION

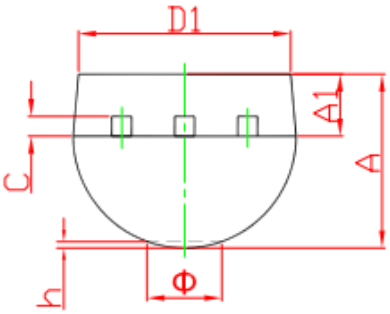
5.1 TO-92 package

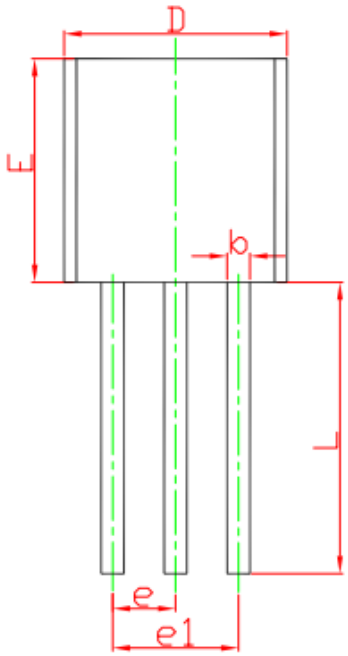


TO-92
NS18B20

PIN	NAME	FUNCTION
1	GND	Ground
2	DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode
3	VDD	Optional VDD. VDD must be grounded for operation in parasite power mode.

TO-92 PACKAGE OUTLINE DIMENSIONS





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
D1	3.430		0.135	
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571
Φ		1.600		0.063
h	0.000	0.380	0.000	0.015

6. ORDER INFORMATION

Orderable Device	Package Type	Marking Information	Description
NS18B20-QTOS	1000ea/Bag	NS18B20	TO-92 package, Plastic Bag

7. OPERATION EXAMPLES

7.1 NS18B20 OPERATION EXAMPLE 1

In this example there are multiple NS18B20s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific NS18B20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	NS18B20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends NS18B20 ROM code.
Tx	44h	Master issues Convert T command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (tCONV).
Tx	Reset	Master issues reset pulse.
Rx	Presence	NS18B20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends NS18B20 ROM code.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

7.2 NS18B20 OPERATION EXAMPLE 2

In this example there is only one NS18B20 on the bus and it is using parasite power. The master writes to the T_H, T_L, and configuration registers in the NS18B20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	NS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	4Eh	Master issues Write Scratchpad command.
Tx	3 data bytes	Master sends three data bytes to scratchpad (TH, TL, and config).
Tx	Reset	Master issues reset pulse.
Rx	Presence	NS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
Tx	Reset	Master issues reset pulse.
Rx	Presence	NS18B20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	48h	Master issues Copy Scratchpad command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

8. REVISION HISTORY

REVISION	DESCRIPTION	REVISION DATE
1.0	initial version	2020/4/10