USB D+/D- Hi-Speed or SBU1/2 Switch with Fault Protection

Features

- Operating Range: 2.7V to 5.5V
- For USB D+/D- Hi-Speed or SBU1/2 signals
- USB Hi-Speed Dual SPDT Switch/MUX
  - Reverse blocking back-to-back MOSFETs
  - >1GHz -3db Bandwidth
  - Low 6Ω Switch On-Resistance
  - Typical 4.0pF Switch On-Capacitance
- Overvoltage Protection
  - Up to +20VDC
  - Surge Protection Up to +25V
- $\overline{\text{FLAG}}$ open drain output overvoltage indicator
- $\overline{\text{EN}}$ to disable switch output
- WLCSP34-12 package (1.17mm x 1.57mm)
- -40°C to +85°C Temperature Range

Applications

- Smartphones
- USB Type-C
- Mobile Internet Devices
- Tablet Computers
- Peripherals

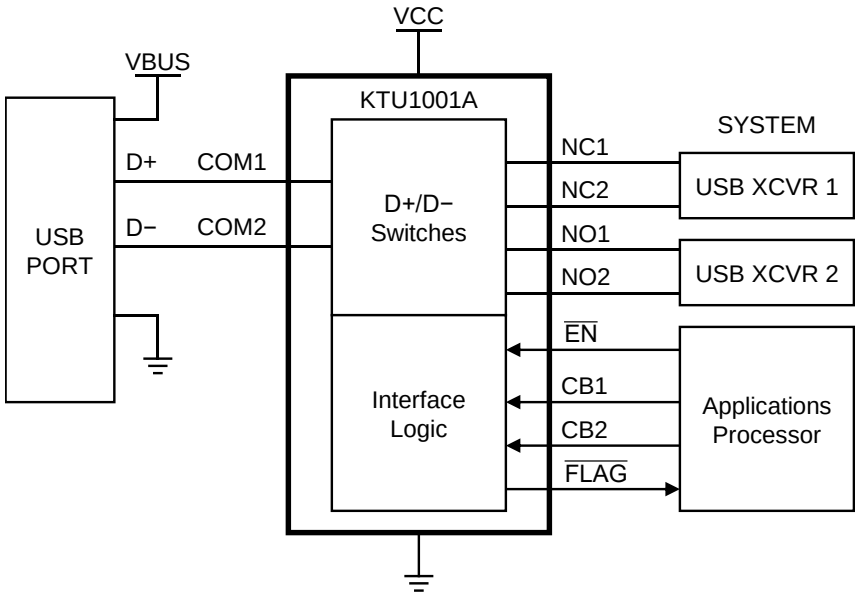
Brief Description

The KTU1001A is a Hi-Speed (up to 480Mbps) USB dual SPDT (single-pole/double-throw) switch with overvoltage protection. This device operates over a 2.7V to 5.5V input supply range with over voltage fault protection up to 20V. USB Type-C features high voltage charging where the KTU1001A protects USB data lines from short circuit and surge events that can permanently damage the mobile system. The device features independent control bits for each switch pair and an on/off enable ($\overline{\text{EN}}$) for shutdown mode. Additional features include low switch on resistance and capacitance along with a fault flag ($\overline{\text{FLAG}}$) to alert the system processor to overvoltage fault events.

Similar in features and performance to KTU1000, the KTU1001A adds reverse blocking MOSFET switch functionality.

The KTU1001A has low power consumption and is available in an ultra-small 12-Bump 1.17mm x 1.57mm WLCSP package making it an ideal solution for USB interface switching and protection in mobile applications.

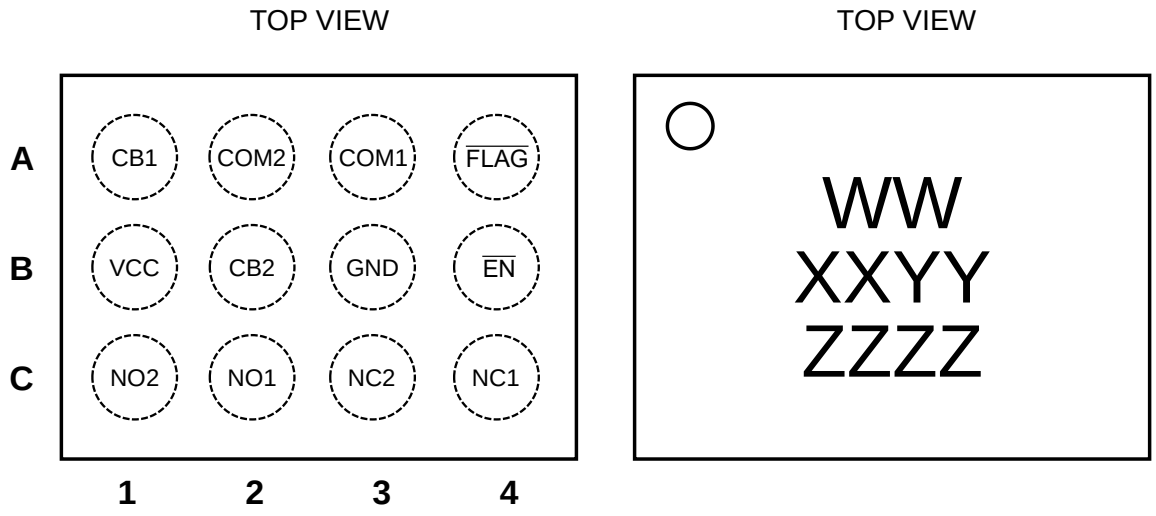
Typical Application



Pin Descriptions

Pin #	Name	Function
A1	CB1	Digital Control Input 1
A2	COM2	Common Terminal for I/O Switch 1 (Connect to D+, D-, SBU1 or SBU2)
A3	COM1	Common Terminal for I/O Switch 2 (Connect to D-, D+, SBU1 or SBU2)
A4	$\overline{\text{FLAG}}$	Active low fault flag output signal to alert fault event
B1	VCC	Input Supply Voltage input pin
B2	CB2	Digital Control Input 2
B3	GND	Ground. Connect this pin to system ground.
B4	$\overline{\text{EN}}$	Active low enable input. Drive EN to a logic high level to disable the device and place switches to a high impedance state.
C1	NO2	Normally Open Terminal for USB I/O Switch 2
C2	NO1	Normally Open Terminal for USB I/O Switch 1
C3	NC2	Normally Closed Terminal for USB I/O Switch 2
C4	NC1	Normally Closed Terminal for USB I/O Switch 1

WLCSP34-12



12-Bump 1.17mm x 1.57mm x 0.62mm
WLCSP Package

Top Mark

WW = Device ID Code = LQ
XX = Date Code, YY = Assembly Code
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VCC	Input voltage	-0.3 to 8	V
CB1, CB2, EN, FLAG	CB1, CB2, EN, FLAG	-0.3 to 6	V
COM1, COM2	I/O Voltage (2.7V < Vcc < 5.5V)	-1 to 20	V
	Surge IEC61000-4-5	25	
NO1, NO2, NC1, NC2	I/O Voltage	-0.7 to 6	V
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C
I_{SW}	Switch I/O Current (Continuous)	25	mA
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

Thermal Capabilities

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient[2]	74	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1697	mW

Ordering Information

Part Number	Marking[3]	Operating Temperature	Package
KTU1001AEVA-TR	LQXXYYZZZZ	-40°C to +85°C	WLCSP-12

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
3. "XXYYZZZZ" is the date code, assembly code and serial number.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typical* values are specified at room temperature (25°C). Vcc = 2.7V to 5.5V.

Symbol	Description	Conditions	Min	Typ	Max	Units
General Operating Conditions						
V_{CC}	Input operating range		2.7		5.5	V
V_{SW}	Analog V_{IO} Signal Range	Vcc = 2.7V to 5.5V	-0.5		V_{FP}	V
V_{UVLO}	Under Voltage Lockout Threshold			2.0	2.5	V
I_{CC}	Supply Current	V_{CC} = 3.0V, $V_{EN\backslash}$ = V_{CC}		0.1	1	µA
		V_{CC} = 3.0V, V_{CB} = Vcc, $V_{EN\backslash}$ = 0V		25	35	µA
V_{FP}	COM Overvoltage Detect Threshold	V_{CC} = 3.0V, VIN rising	4.5	4.8	5.1	V
		V_{CC} = 3.0V, VIN falling		4.3		V
t_{FP}	Fault Protection Response Time	V_{COM} = 1V to 10V step, Vcc = 3.0V; Figure 1			100	ns
t_{FPR}	Fault Protection Recovery Time	V_{COM} = 10V to 1V step, Vcc = 3.0V; Figure 1		26		us
R_{ON}	On-Resistance	V_{COM} = 0V to V_{CC}, $I_{COM\_}$ = 10mA		6.0	9.0	Ω
$R_{ON[MATCH]}$	On-Resistance Match between channels	V_{COM} = 0V to V_{CC}, $I_{COM\_}$ = 10mA			0.3	Ω
$R_{ON[FLAT]}$	On-Resistance Flatness	V_{COM} = 0V to V_{CC}, $I_{COM\_}$ = 10mA			0.45	Ω
$I_{COM\_(OFF)}$	COM_ Off Leakage Current	V_{CC} = V_{EN} = 3.0V, V_{COM} = 3.0V or 0V, V_{NC} = 0V or 3.0V		0.5	10	µA
$R_{COM\_(GND)}$	COM_ Isolation Resistance to GND when switch is on	V_{CC} = 3.0V, V_{EN} = 0V, V_{COM} = 3.0V or 0V, Ta = 25°C	4.1	5.5	6.9	MΩ
$I_{NC\_(OFF)}$	NC_ Off Leakage Current	V_{CC} = V_{EN} = 3.0V, V_{COM} = 3.0V or 0V, V_{NC} = 0V or 3.0V		±0.1	±1	µA
Timing – Figures 2 and 3						
$t_{ON[WAKEUP]}$	IC Wake-Up Turn On Time	V_{CC} = 3.0V, V_{COM} = 1.5V, R_L=50Ω, V_{EN} = 0V, V_{CB} = 0V to V_{CC}, Figure 3		14	30	µs
$t_{ON[SW]}$	SW Transition Turn On Time	V_{CC} = 3.0V, V_{COM} = 1.5V, R_L=50Ω, V_{EN} = 0V, V_{CB} = 0V to V_{CC}, Figure 2a		28	60	µs
$t_{OFF[SW]}$	SW Transition Turn Off Time	V_{CC} = 3.0V, V_{COM} = 1.5V, R_L = 50Ω, V_{EN} = 0V, V_{CB} = 0V to V_{CC}, Figure 2a		1		µs
t_D	Break-Before-Make Time Delay	R_L = 50Ω		28		µs
$C_{COM(OFF)}$	Off Capacitance	V_{COM} = 0.5V_{P-P}, DC bias = 0V, f = 1MHz		4.5		pF
$C_{COM(ON)}$	On Capacitance	V_{COM} = 0.5V_{P-P}, DC bias = 0V, f = 240MHz		4		pF
AC Performance						
BW	-3dB Bandwidth	R_S = R_L = 50Ω, V_{COM} = 0dBm		>1		GHz
V_{ISO}	Off Isolation	f = 100kHz, V_{COM} = 0.5V_{p-p}, R_S = R_L = 50Ω		-70		dB
V_{CT}	Crosstalk	f = 100kHz, V_{COM} = 0.5V_{p-p}, R_S = R_L = 50Ω		-80		dB
Logic Input, Enable, CB1, CB2						
V_{IH}	Input Logic High		1.2			V
V_{IL}	Input Logic Low				0.4	V
I_{LK_IN}	Input Leakage Current	$\overline{EN}$ = CB_ = 0V or V_{CC}	-1		1	µA
Fault Flag						
V_{OL}	$\overline{FLAG}$ Output Voltage Low	V_{IO} = 3.3V, I_{SINK} = 1mA		0.1	0.4	V
I_{LK_OUT}	$\overline{FLAG}$ Output Leakage Current	V_{IO} = 3.3V, $\overline{FLAG}$ de-asserted	-1		1	µA

4. KTU1001A is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Timing Diagrams

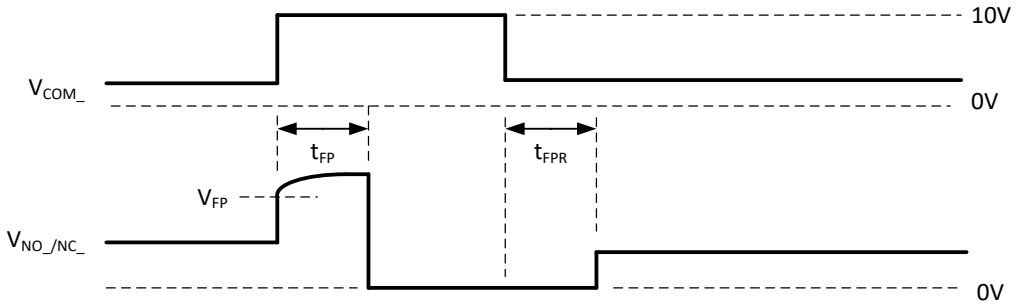


Figure 1. Fault Protection Timing Diagram

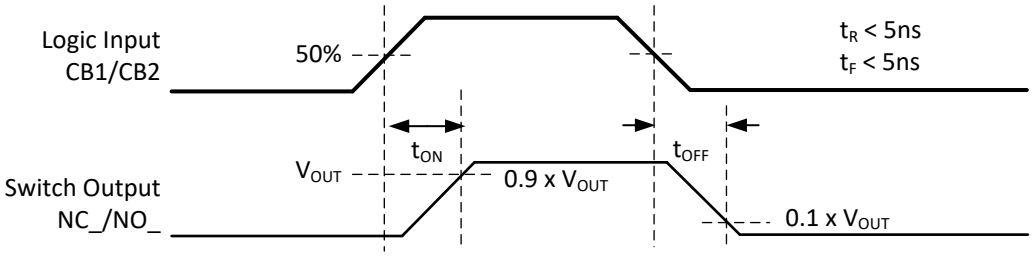


Figure 2a. USB COM1/2 On – Off Switch Control Timing Diagram

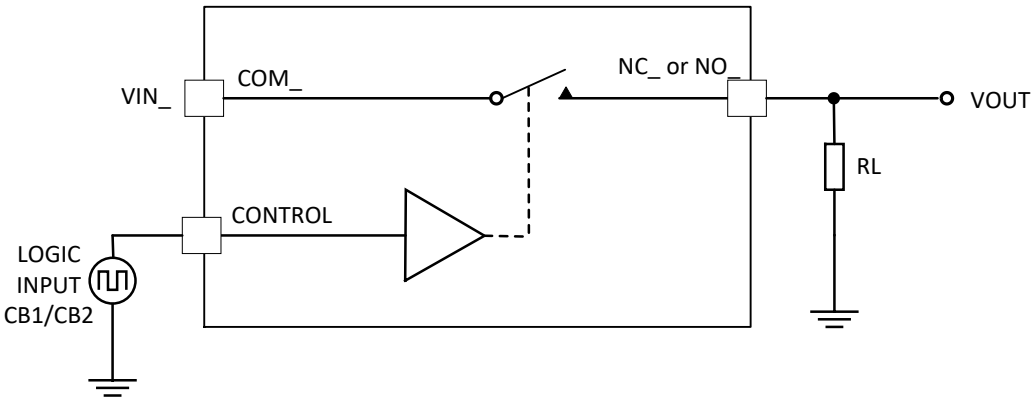


Figure 2b. Switch Timing Test Circuit

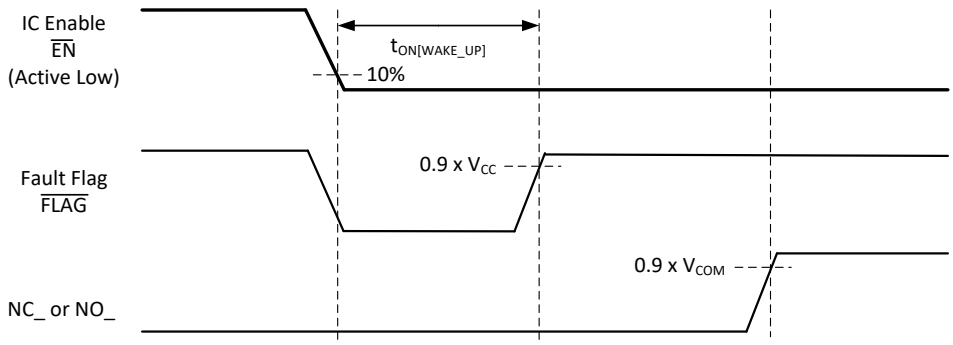


Figure 3. IC Wake-Up Timing Diagram

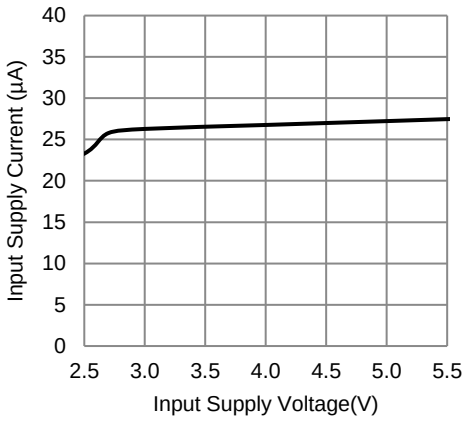
Enable and Control Input Truth Table

Control Logic Inputs			Switch Status	
$\overline{EN}$	CB1	CB2	COM1	COM2
0	0	0	NC1	NC2
0	0	1	NC1	NO2
0	1	0	NO1	NC2
0	1	1	NO1	NO2
1	X	X	OPEN	OPEN

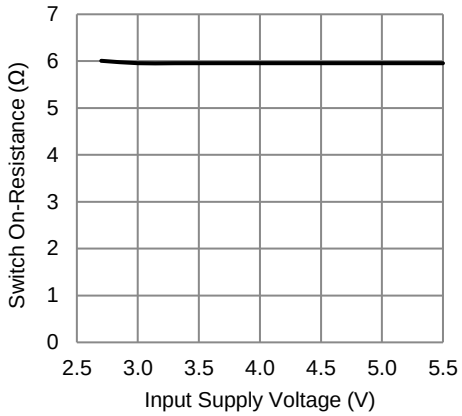
Typical Characteristics

VCC = 3V, C_{VCC} = 1µF, T_{AMB} = 25°C unless otherwise specified.

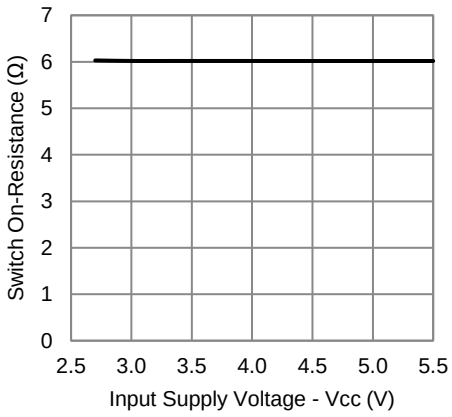
Input Supply Current vs Input Supply Voltage



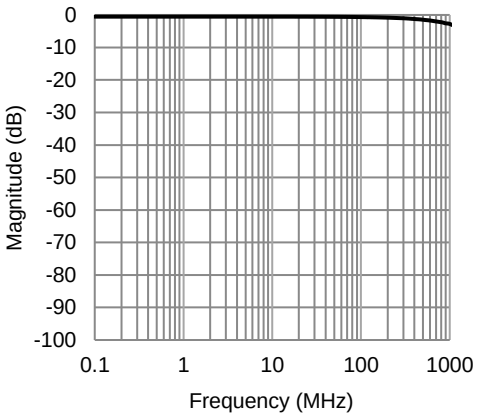
Switch On-Resistance vs COM Voltage



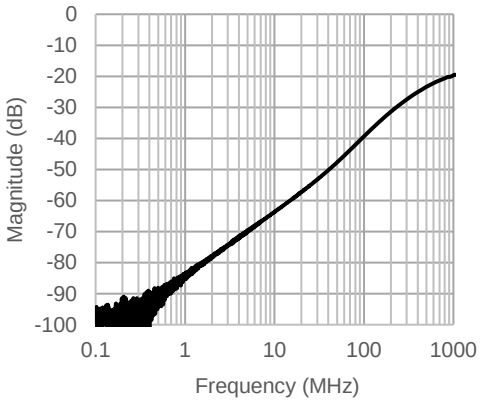
Switch On-Resistance vs Input Supply Voltage



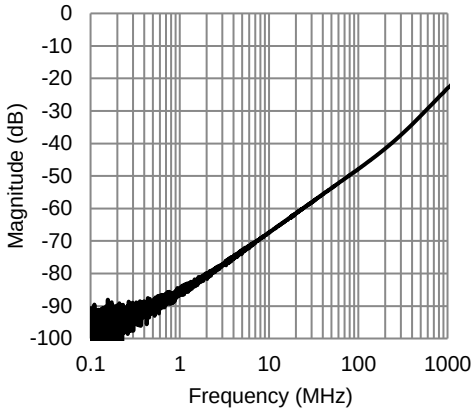
Frequency Response - On Loss



Frequency Response - Off Isolation



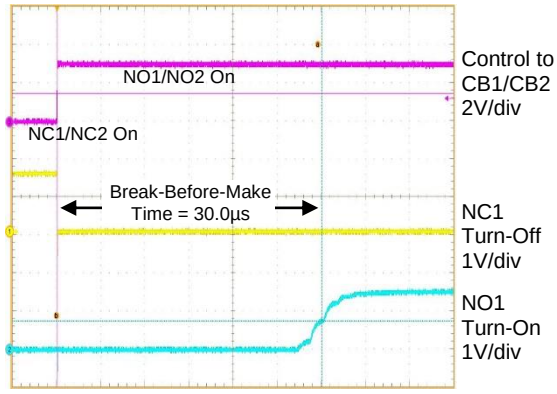
Frequency Response - Crosstalk



Typical Characteristics (continued)

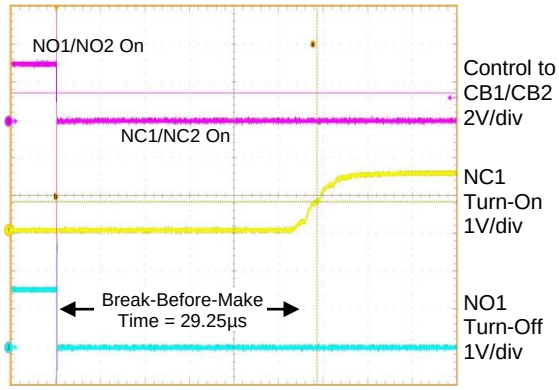
VCC = 3V, C_{VCC} = 1µF, T_{AMB} = 25°C unless otherwise specified.

NC1 to NO1 Switch Break-Before-Make Timing



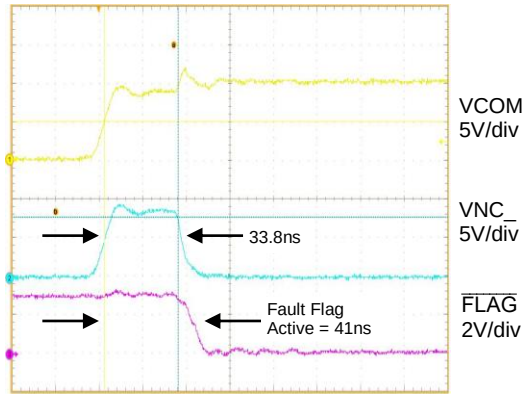
5µs/div

NO1 to NC1 Switch Break-Before-Make Timing



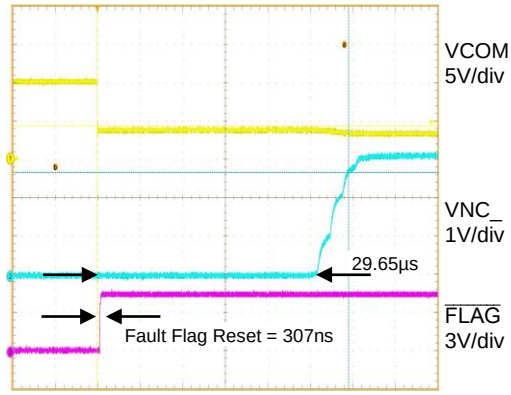
5µs/div

COM Input OVP to NC/NO Output Shutdown Fault Flag Reporting Time



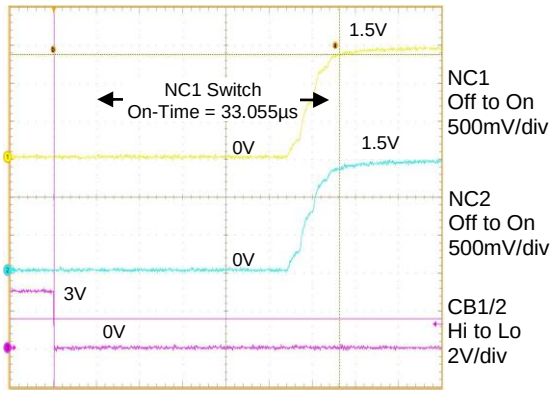
20ns/div

COM Input OVP to NC/NO Output Recovery Time



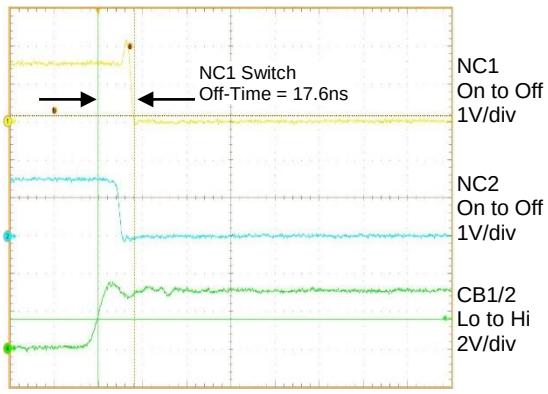
5µs/div

Switch On-Time



5µs/div

Switch Off-Time

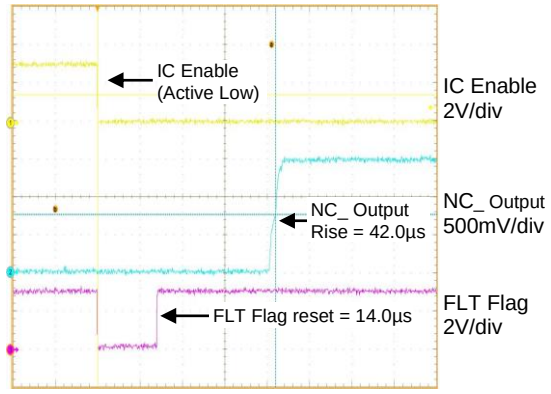


20ns/div

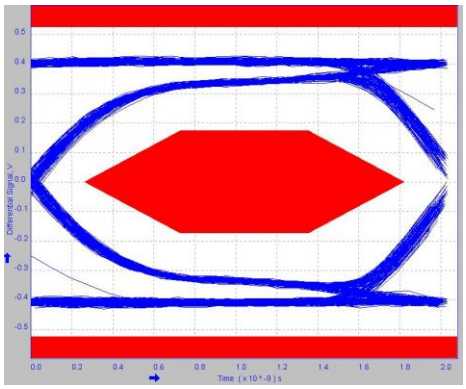
Typical Characteristics (continued)

VCC = 3V, C_{VCC} = 1µF, T_{AMB} = 25°C unless otherwise specified.

IC Turn-On Time From Enable



Eye Diagram USB 2.0 High-Speed



Functional Block Diagram

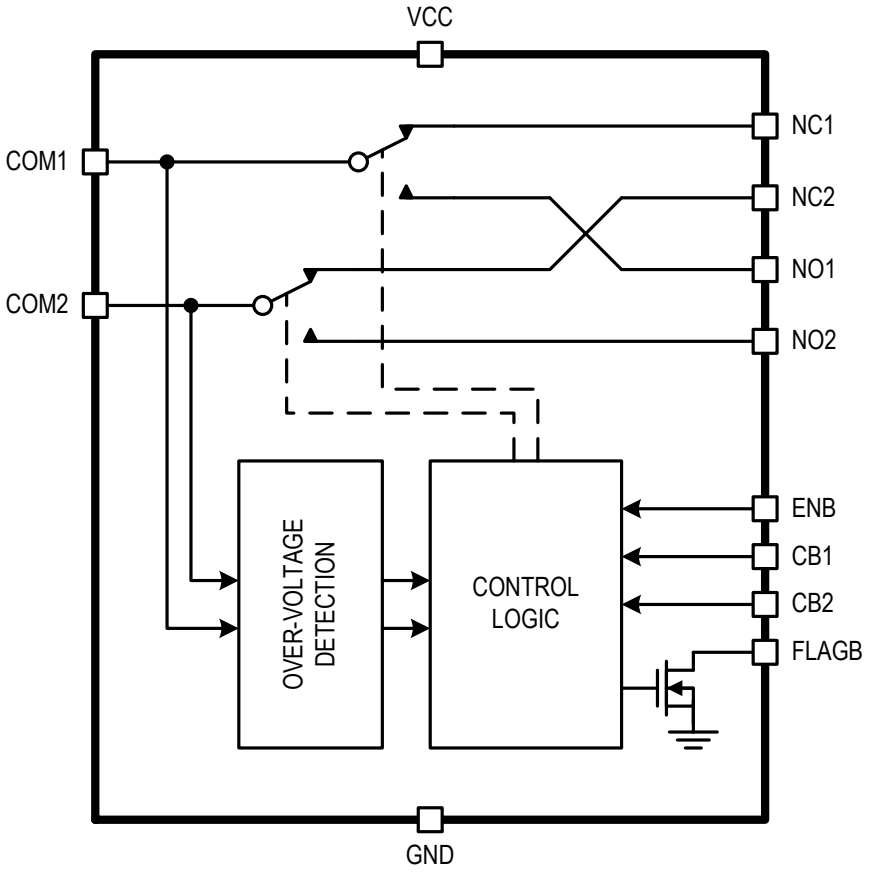


Figure 4. Functional Block Diagram

Functional Description

The KTU1001A is a DPDT analog switch intended for 2:1 MUX operation for USB 2.0 Low (LS), Full (FS), High Speed (HS) and Display Port AUX channel applications. This device is specified to operate over a 2.7V to 5.5V input supply range. An active logic low enable pin ($\overline{EN}$) along with two switch state control pins (CB1 and CB2) provide full control of IC functions. When the device is disabled, the quiescent current consumption drops to less than 1µA. Upon IC enable, supply quiescent current increases to a typical 25µA to save power in battery powered portable products. The default enable DPDT switch state is normally closed between the COM1/2 pins and the NC1/2 pins unless otherwise programmed via the CB1/2 pins. Refer to the IC control truth table for all programming logic states.

The NC_ and NO_ switch pairs utilize break-before-make switching to assure the COM1/2 inputs are only passed to one switch output pair at any given time. When switch pairs are toggled to the opposite output via the CB1/2 control pins, the on-switch will open with a typical 28µs delay before the off-switchs close.

The USB switch inputs COM1 and COM2 are over voltage protected with fixed typical OVP threshold level at 4.8V regardless of the applied Vcc supply voltage. Should a voltage level greater than the OVP threshold be applied to either COM1 or COM2, the IC will disable the switches to NC_ or NO_ and place them in a high impedance state to protect the device and down steam USB controller from damage. An active-low fault flag output ($\overline{FLAG}$) is provided to alert the system controller to the fault condition.

Application Information

Analog Switch Applications

The KTU1001A is intended for use as a USB 1:2 data mux for USB 2.0 Low, Full and Hi-Speed applications up to 480Mbps and has an analog bandwidth up to 1GHz. KTU1001A switches may be used for other AC coupled analog signal switching applications as long as applied signal levels are within the minimum to maximum V_{SW} operating limits as defined in the electrical characteristics specification for this device. Due to the high frequency nature of USB and similar data signals, unused switch inputs or output should be terminated with 50Ω to ground to prevent unwanted signal-line reflections.

Reverse-Blocking Switches

The switches in the KTU1001A are reverse-blocking, using back-to-back MOSFET switches in each path. When the switches are OFF, current is blocked in both directions from NO1, NO2, NC1, or NC2 to COM1 or COM2. This allows more system flexibility for USB transceivers or other I/O devices connected in the system, it is not necessary to control the state of disabled channels NO1, NO2, NC1, or NC2.

For lower Rdson and capacitance, please refer to KTU1000.

Input Supply Bypass Capacitor

The KTU1001A may be operated with no additional external components. To maximize Hi-Speed data performance in systems with voltage supply noise or ripple, adding a Vcc input bypass capacitor in the range of 0.1µF or 1µF from V_{CC} to GND is recommended. Ceramic capacitors with minimum voltage rating of 6.3V and X5R or X7R dielectric should be used.

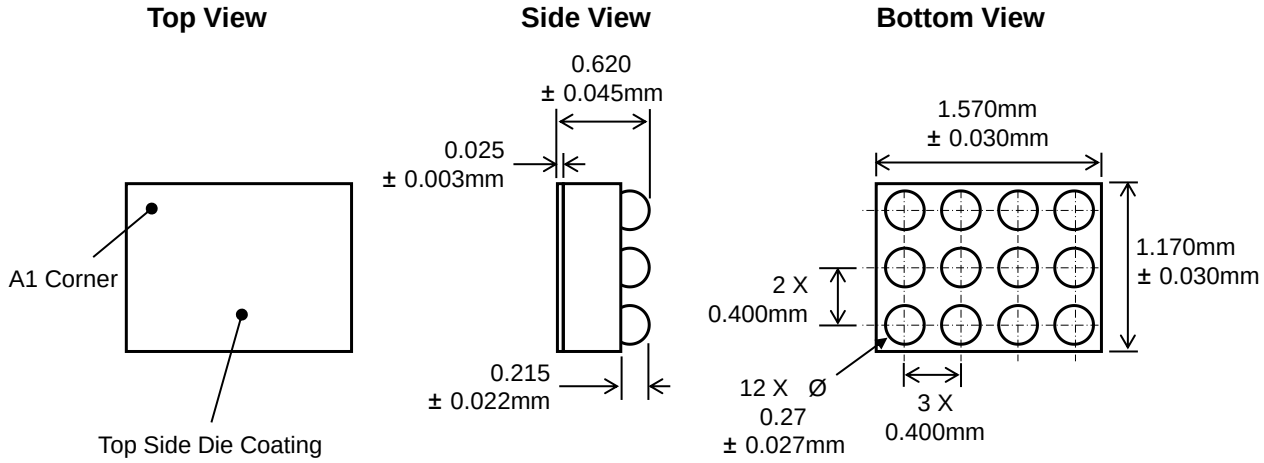
PCB Layout Guidelines

To achieve adequate bandwidth in USB 2.0 Hi-Speed data applications, careful PCB layout is critical for the signal traces to the COM1, COM2, NC1, NC2, NO1, and NO2 pins. The following guidelines are recommended for best system performance:

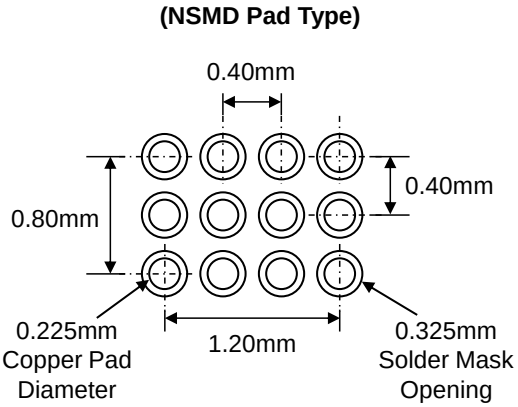
1. Multi-layer printed circuits boards are recommended for hi-speed data communication applications. Best USB signal quality is realized with 4 layer or greater PCB assemblies. A multilayer board minimizes the board material thickness between the signal trace layer and adjacent ground plane layer, which aids in maintaining consistant trace impedance for high-frequency signals.
2. Input and Output data signals should utilize matched width and length traces and be made as short as possible. As a general guide, USB 2.0 Hi-Speed signals, traces should be equal in lengths, maintain a 6 mil width with 8 mil spacing between traces and have 30 mil or greater isolation to adjacent signal traces.
3. The use of data trace vias should be minimized or ideally avoided altogether as they introduce impedance discontinuities at high frequencies and compromise signal quality.
4. If signal traces require turns or bends, do not use 90° turns. To maintain good high frequency performance, trace turns should use rounded arcs or bend at 45° angles at a maximum.
5. All signal traces should be routed directly over ground planes placed on the next PCB layer. To maintain best PCB trace impedance characteristic and minimize electro-magnetic interfearance (EMI), the ground plane layer should have no breaks under the signal trace layer. The ground plane layer should be referenced back to the system power source ground at one single point to avoid stray current paths through the ground plane.

Packaging Information

WLCSP34-12 (1.570mm x 1.170mm x 0.620mm)



Recommended Footprint



* Dimensions are in millimeters.