

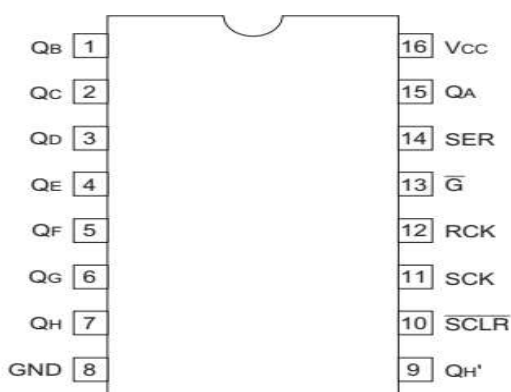
Description

The XL74HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state. The XD74LS595 characterized for operation from 0 °c to 70 °c

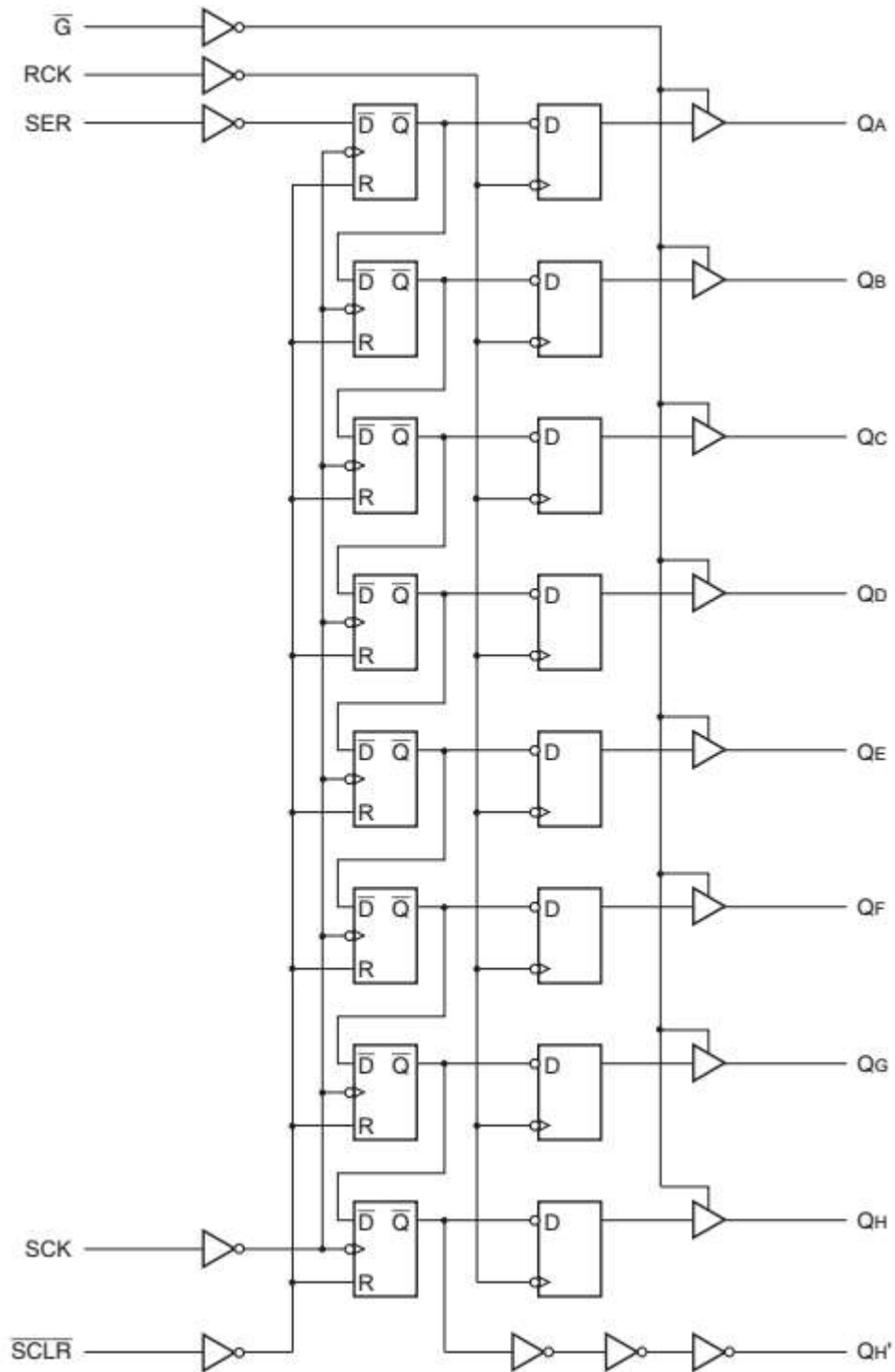
Function Table

Inputs				Function
RCK	SCK	$\overline{\text{SCLR}}$	$\overline{\text{Q}}$	
X	X	X	H	Q_A to Q_H high impedance
X	X	L	X	Shift register cleared $Q_H' = L$
X	\square	H	X	Shift register clocked $Q_n = Q_{n-1}$, $Q_A = \text{SER}$
\square	X	H	X	Contents of shift register transferred to output latches

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	0°C to 70°C	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = 0^\circ\text{C to } 70^\circ\text{C}$		Unit	Test Conditions				
			Min	Typ	Max	Min	Max						
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V					
		4.5	3.15	—	—	3.15	—						
		6.0	4.2	—	—	4.2	—						
	V_{IL}	2.0	—	—	0.5	—	0.5				V		
		4.5	—	—	1.35	—	1.35						
		6.0	—	—	1.8	—	1.8						
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Q_A to Q_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$			
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -6\ \text{mA}$			
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -7.8\ \text{mA}$			
		4.5	4.18	—	—	4.13	—						
		6.0	5.68	—	—	5.63	—						
		6.0	5.68	—	—	5.63	—						
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Q_A to Q_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$			
		4.5	—	0.0	0.1	—	0.1						
		6.0	—	0.0	0.1	—	0.1						
		4.5	—	—	0.26	—	0.33			$I_{OL} = 6\ \text{mA}$			
		6.0	—	—	0.26	—	0.33			$I_{OL} = 7.8\ \text{mA}$			
		6.0	—	—	0.26	—	0.33						
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Q'_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$			
		4.5	4.4	4.5	—	4.4	—						
		6.0	5.9	6.0	—	5.9	—						
		4.5	4.18	—	—	4.13	—			$I_{OH} = -4\ \text{mA}$			
		6.0	5.68	—	—	5.63	—			$I_{OH} = -5.2\ \text{mA}$			
		6.0	5.68	—	—	5.63	—						
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Q'_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$			
		4.5	—	0.0	0.1	—	0.1						
		6.0	—	0.0	0.1	—	0.1						
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\ \text{mA}$			
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\ \text{mA}$			
		6.0	—	—	0.26	—	0.33						
Off-state output current	I_{OZ}	6.0	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH}$ or V_{IL} , $V_{out} = V_{CC}$ or GND				
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND				
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0\ \mu\text{A}$				

8-Bit Shift Registers With 3-State Output Registers

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = 0^\circ\text{C to } 70^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	31	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	115	—	145	ns	SCK to Q_H'
		4.5	—	12	23	—	29		
		6.0	—	—	20	—	25		
	t_{PHL}	2.0	—	—	150	—	190	ns	RCK to Q
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH}	2.0	—	—	175	—	220	ns	$\overline{\text{SCLR}}$ to Q_H'
		4.5	—	20	35	—	44		
		6.0	—	—	30	—	37		
Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	SER to SCK
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	200	—	—	250	—	ns	SCK to RCK
		4.5	40	8	—	50	—		
		6.0	34	—	—	43	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	1	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	Q_H'
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
	t_{THL}	2.0	—	—	60	—	75	ns	Q
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	5	pF	

Ordering information

PN:	Package
XL74HC595	SOP16 2,500Pcs/Reel

SOP16 Dimension

