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# SPECIFICATION

## Revision 0.1

### AT070DP50-A

<b>Customer</b>	
<b>Model NO.</b>	<b>AT070DP50-A</b>
<b>Product Type</b>	<b>TFT 7.0 inch, 800*RGB*480 dots matrix</b>
<b>Remarks</b>	
<b>Signature by Customer:</b>	

<b>Issued by</b>	<b>Checked by</b>	<b>Approved by</b>	<b>Approved by</b>
		<b>R&amp;D</b>	<b>QA</b>



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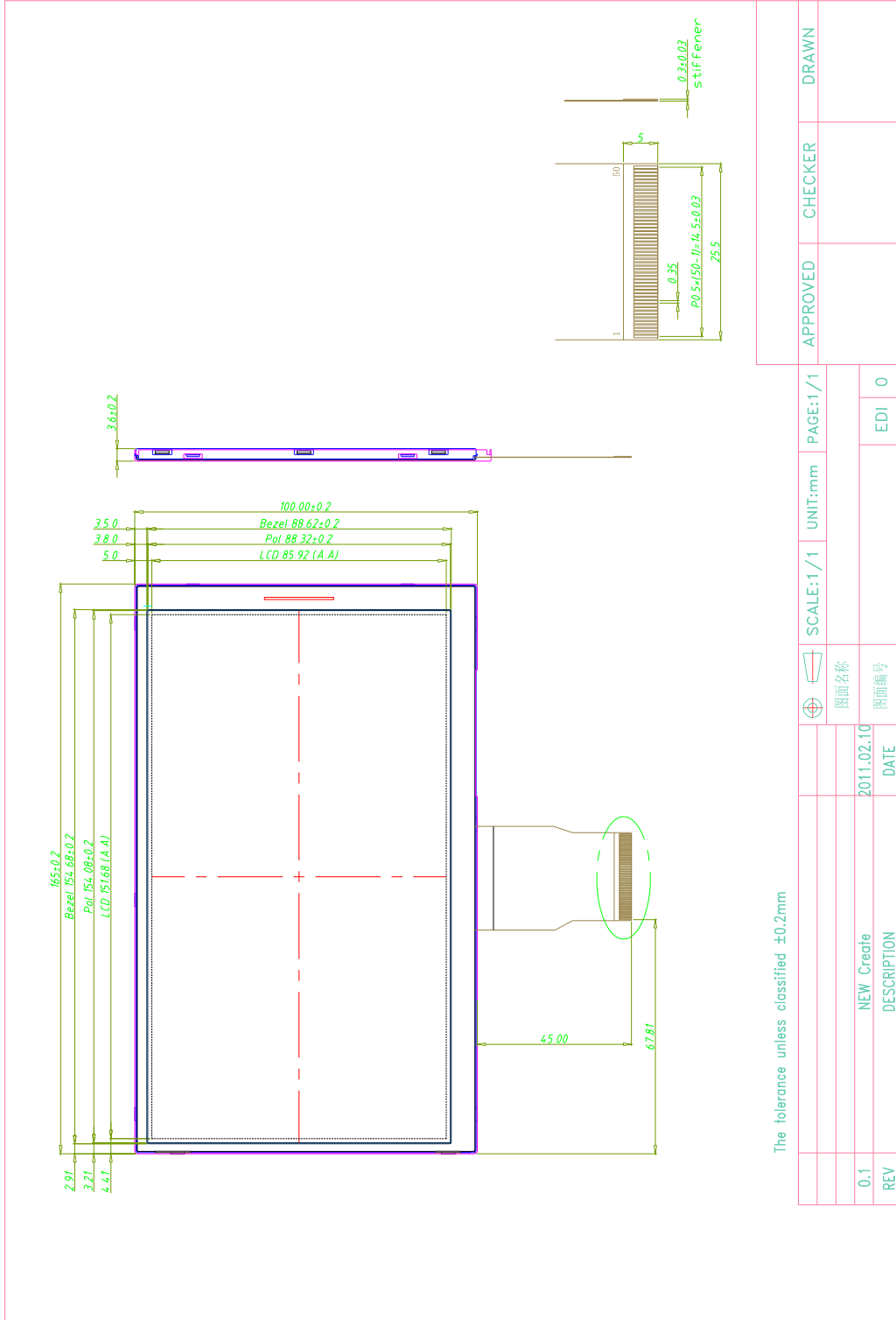
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<b>Item</b>	<b>Contents</b>
LCD type	TFT transmissive
Viewing direction	12 O'Clock
Outline area(W*H)	165.0mm *100.0mm*3.6(T)
Active area(W*H)	151.68mm * 85.92mm
Number of dots	800*RGB*480
Response Time(Tr+Tf)	25ms(typ)
Colors	16.2M
Interface type	System parallel interface
Input voltage	3.3V

## ■ External Dimensions



图面名称	图面编号	SCALE: 1/1	UNIT:mm	PAGE: 1/1	APPROVED	CHECKER	DRAWN
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■ Absolute Maximum Ratings

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Parameter	Symbol	Min.	Max.	Unit
Digital Supply Voltage	DVDD	-0.3	+5.0	V
Analog Supply Voltage	AVDD	-0.5	+13.5	V
Gate On Voltage	VDDG	-0.3	+42	V
Gate Off Voltage	VEEG	-20	+0.3	V
Gate On-Gate Off Voltage	VDDG-VEEG	12	40	V
Operating temperature	Vop	-20	70	°C
Storage temperature	Tst	-30	80	°C

## ■ Electrical Characteristics

Parameter	Symbol	Min.	Type.	Max.	Unit.	Note.
Digital Supply Voltage	DVDD	3.0	3.3	3.6	V	
Analog Supply Voltage	AVDD	9.4	9.6	9.8	V	
Gate On Voltage	VDDG	17	18	19	V	
Gate Off Voltage	VEEG	-6.6	-6	-5.4	V	
Common Voltage	VCOM	3.8	4	4.2	V	Note1
Logic input Voltage	VIH	0.7VDD	-	VDD-	V	
	VIL	GND	-	0.3VDD	V	

Note 1: Please adjust VCOM to make the flicker level be minimum

## ■ Current consumption

Parameter	Symbol	Min.	Type.	Max.	Unit.	Note.
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Gate On Current	IVDDG	-	0.5	1	mA	
Gate Off Current	IVEEG	-	0.5	1	mA	
Digital Current	IDVDD	-	8	15	mA	
Analog Current	IAVDD	--	30	40	mA	

## ■ Backlight Characteristics

Item	Symbol	Min.	Type	Max.	Unit	Condition
Forward voltage	Vf	12.0	12.8	13.2	V	If=120mA
Luminance	Lv	230	250	300	Cd/m <sup>2</sup>	Ta=25°C
Number of LED	-	18			Piece	-
Connection mode	P	0.8IOVcc	-	IOVcc	V	-

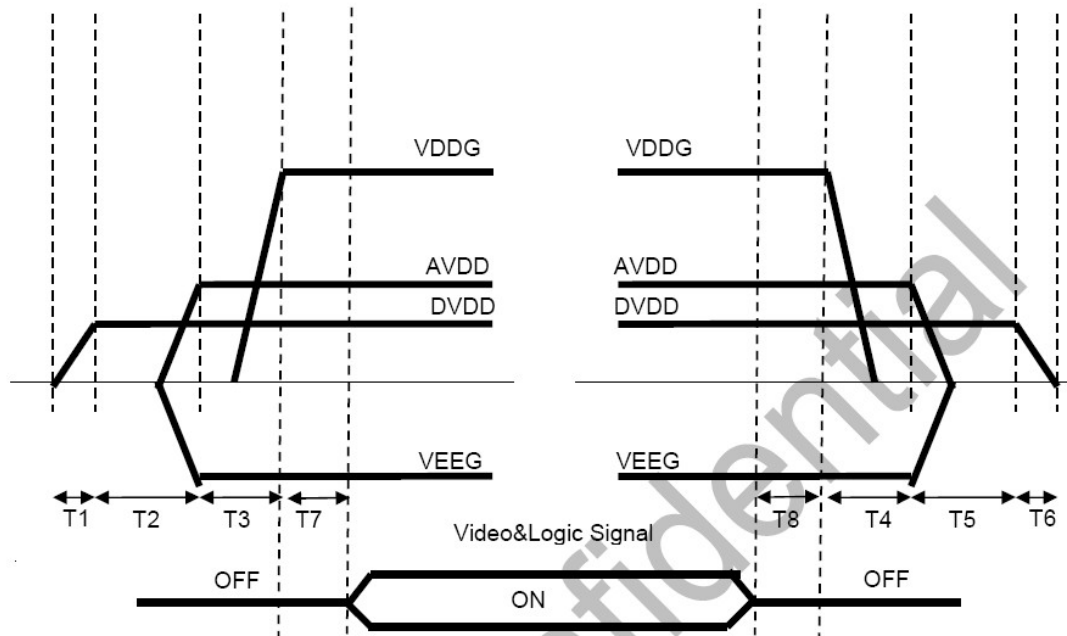
## ■ Timing of Power Supply

### Power Signal sequence

Power On: DVDD→AVDD/VEEG→VDDG→Video & Logic Signal

Power Off: Video & Logic Signal→VDDG→AVDD/VEEG→VDD

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$$\begin{aligned}
 0 < T1 &\leq 10\text{ms} & T5 &> 0\text{ms} \\
 T2 &> 20\text{ms} & T6 &> 0\text{ms} \\
 T3 &> 10\text{ms} & 0 < T7 &\leq 10\text{ms} \\
 T4 &> 10\text{ms} & 0 < T8 &\leq 10\text{ms}
 \end{aligned}$$

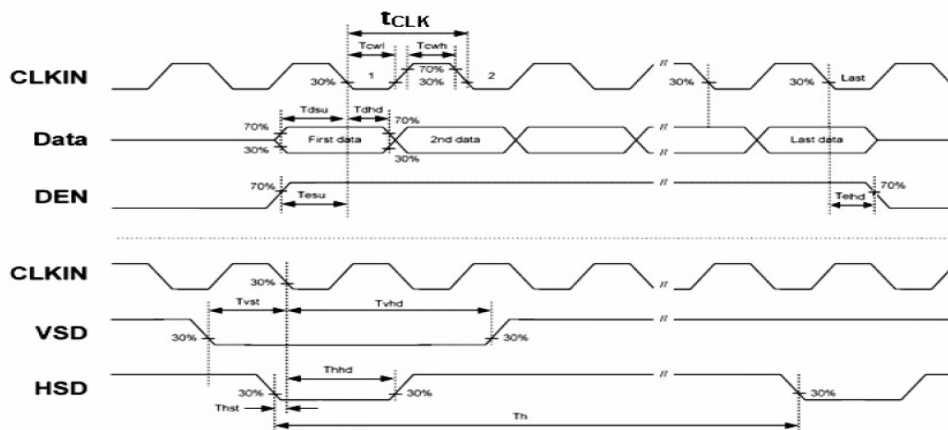
### Timing characteristics of input signals

	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Note
DCLK	Dot Clock	1/tclk	29	33	38	MHz	
	DCLK pulse duty	Tcwh	40	50	60	%	
DE	Setup Time	Tesu	8	-	-	ns	
	Hold time	Tehd	8	-	-	ns	



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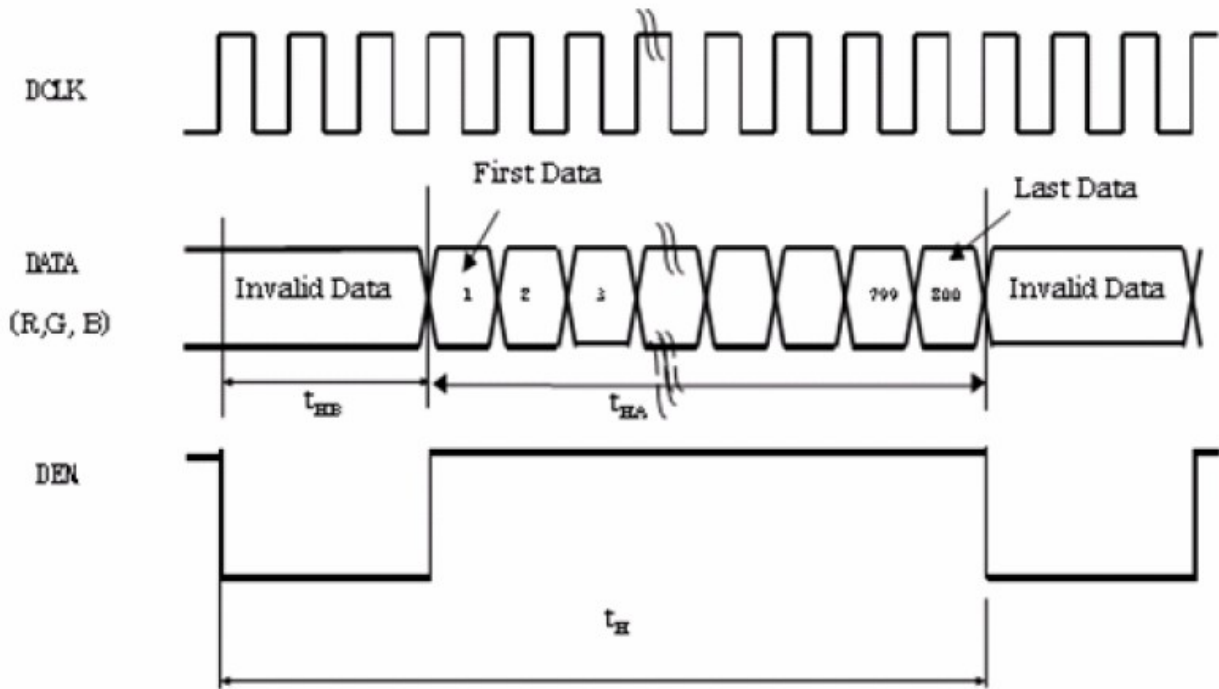
	Horizontal Period	tH	1026	1056	1086	tclk	
	Horizontal Valid	tHA	800			tclk	
	Horizontal Blank	tHB	-	256	-	tclk	
	Vertical Period	tV	515	525	535	tH	
	Vertical Valid	tVA	480			tH	
	Vertical Blank	tVB	-	45	-	tH	
SYNC	HSYNC Setup Time	Thst	8	-	--	ns	
	HSYNC Hold Time	Thhd	8	-	-	ns	
	VSYNC Setup Time	Tvst	8	-	-	ns	
	VSYNC Hold Time	Tvhd	8	-	-	ns	
	Horizontal Period	th	1026	1056	1086	tclk	
	Horizontal Pulse Width	thpw	-	30	-	tclk	
	Horizontal Back Porch	thb	-	16	-	tclk	
	Horizontal Front Porch	thfp	180	210	240	tclk	
	Horizontal Valid	thd	800			tclk	
	Vertical Period	tv	515	525	535	th	
	Vertical Pulse Width	tvpw	-		-	th	
	Vertical Back Porch	tvb	-		-	th	
	Vertical Front Porch	tvfp	12	22	32	th	
	Vertical Vlid	tvd	480			th	
DATA	Setup Time	Tdsu	8	-	-	ns	
	Hold Time	Tdhd	8	-	-	ns	



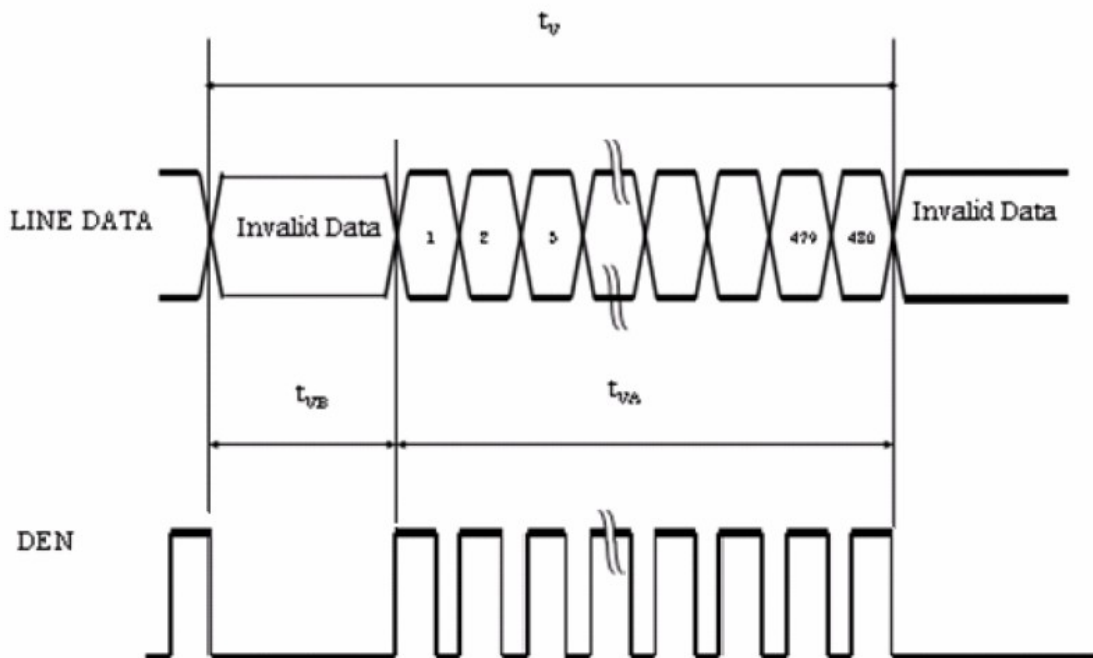
## DE mode

Horizontal timing:

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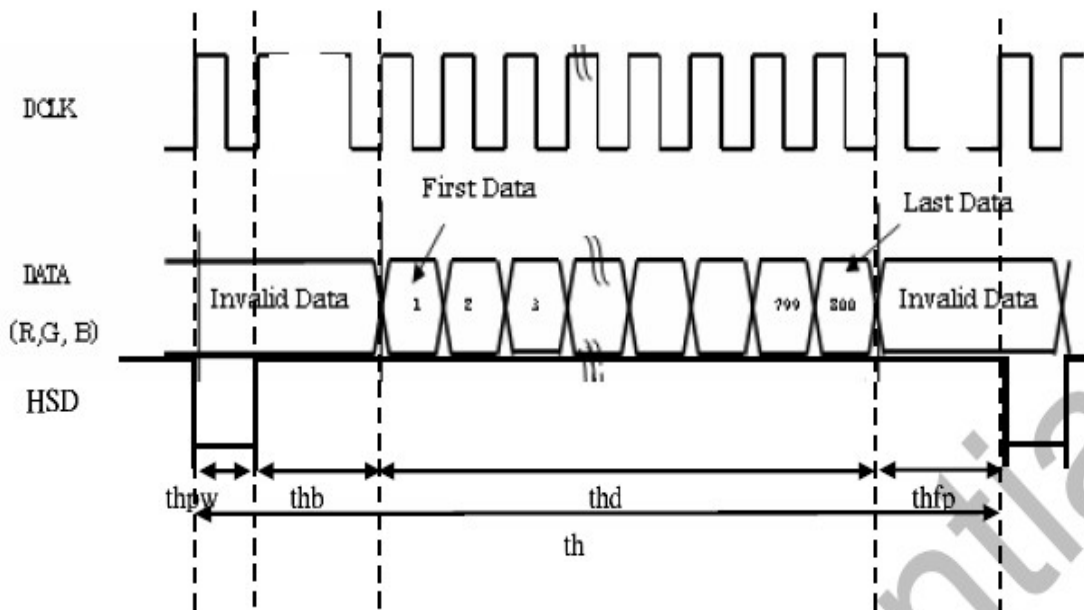


Vertical timing:

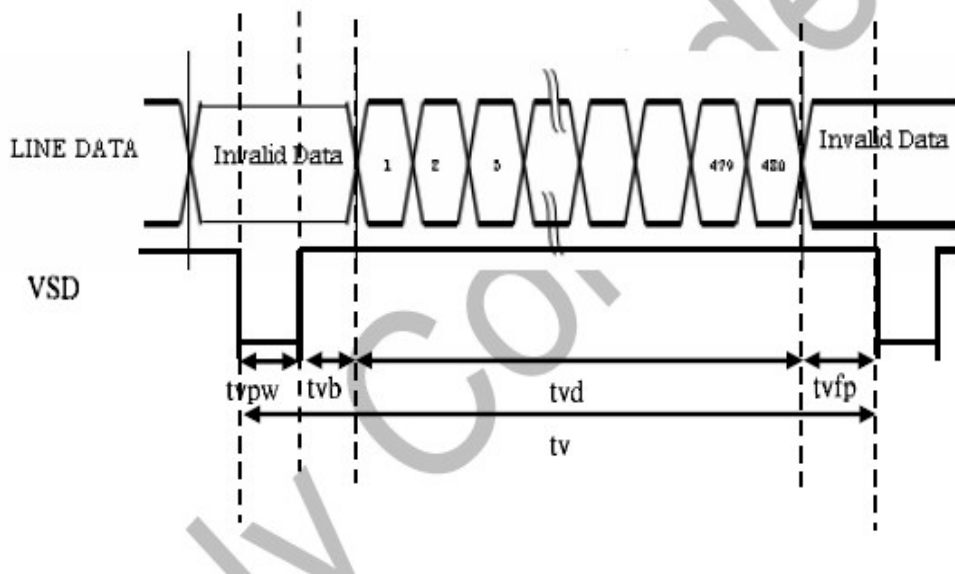


## SYNC mode

Horizontal timing:



Vertical timing :



## Interface Description

Pin NO.	Signal	Function
1	VLED+	Power for LED backlight(Anode)

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2	VLED+	Power for LED backlight(Anode)
3	VLED-	Power for LED backlight(Cathode)
4	VLED-	Power for LED backlight(Cathode)
5	GND	Ground.
6	VCOM	Common Voltage
7	DVDD	Digital Power
8	MODE	DE/SYNC mode select. Normally pull high H: DE mode. L: HSD/VSD mode
9	DE	Data Enable signal
10	VSD	Write signal.
11	HSD	Read signal.
12	B7	Blue Data input(MSB)
13	B6	Blue Data input
14	B5	Blue Data input
15	B4	Blue Data input
16	B3	Blue Data input
17	B2	Blue Data input
18	B1	Blue Data input
19	B0	Blue Data input(LSB)
20	G7	Green Data input(MSB)
21	G6	Green Data input
22	G5	Green Data input
23	G4	Green Data input
24	G3	Green Data input
25	G2	Green Data input
26	G1	Green Data input
27	G0	Green Data input(LSB)
28	R7	Red Data input(MSB)
29	R6	Red Data input
30	R5	Red Data input
31	R4	Red Data input
32	R3	Red Data input
33	R2	Red Data input
34	R1	Red Data input
35	R0	Red Data input (LSB)
36	GND	Power ground
37	DCLK	Clock input
38	GND	Power ground
39	SHLR	Left or Right Display Control
40	UPDN	Up or Down Display Control

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41	VDDG	Positive Power for TFT
42	VEEG	Negative Power for TFT
43	AVDD	Analog Power
44	RSTB	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high.(R=10K,C=1uF)
45	NC	Not connect
46	VCOM	Common Voltage
47	DITH	Dithering setting DITH="H" 6bit resolution(last 2 bit of input data truncated) DITH="L" 8bit resolution(default setting)
48	GND	Power ground
49	NC	Not connect
50	NC	Not connect

**Note 1 SHLR: left or right setting**

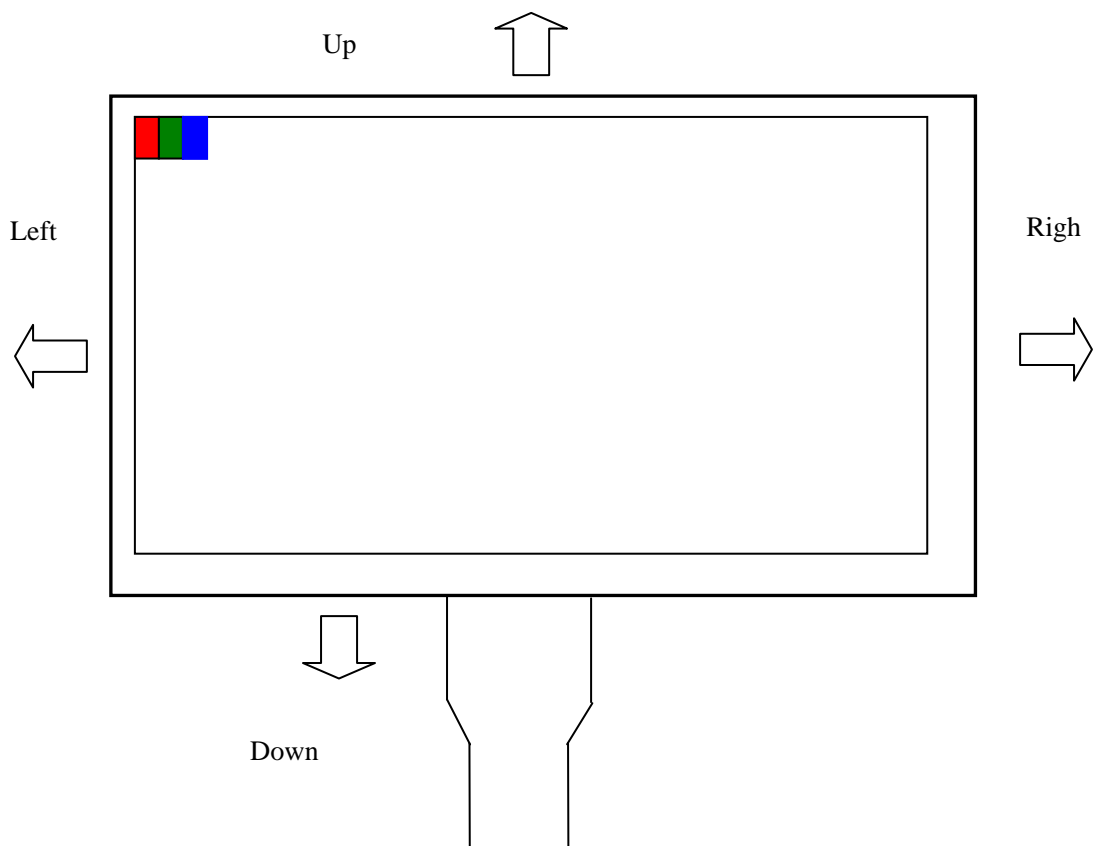
**UPDN: up or down setting**

SHLR	UPDN	Data shifting
VDD	GND	Left→Right, Up→Down(default)
GND	GND	Right→Left, Up→Down

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VDD	VDD	Left→Right, Down→Up
GND	VDD	Right→Left, Down→Up

### Definition of scanning direction.



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### ■ Reliability Test

Test item	Test Condition
High Temperature Storage	60±2°C/48 hours
Low Temperature Storage	-10±2°C/48 hours
High Temperature Operating	45±2°C/48 hours
Low Temperature Operating	0±2°C/48 hours

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Temperature Cycle	0±2℃ ~ 50±2℃ × 10cycles (30min.) (5min.) (30min.)
Damp Proof Test	50℃ ±5℃ ×90%RH/48 hours
ESD test	Voltage: ±4KV R: 330 Ω C:150pF Air discharge, 10time