

FEATURES

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20 years at temperature
- RoHS-compliant small footprint BGA and TSOP2 package
- All products meet MSL-3 moisture sensitivity level



BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM



INTRODUCTION

The MR4A16B is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 1,048,576 words of 16 bits. The MR4A16B offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. To simplify fault tolerant design, the MR4A16B includes internal single bit error correction code with 7 ECC parity bits for every 64 data bits. The MR4A16B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.



The **MR4A16B** is available in a small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOP Type 2). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR4A16B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), and industrial temperature (-40 to +85 °C) operating temperature options.

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1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram



Table 1.1 Pin Functions

| Signal Name | Function |
|-------------|-------------------|
| A | Address Input |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| \bar{UB} | Upper Byte Enable |
| \bar{LB} | Lower Byte Enable |
| DQ | Data I/O |
| V_{DD} | Power Supply |
| V_{SS} | Ground |
| DC | Do Not Connect |
| NC | No Connection |

Figure 1.1 Pin Diagrams for Available Packages (Top View)



48-Pin BGA



54-Pin TSOP2

Table 1.2 Operating Modes

| \bar{E}^1 | \bar{G}^1 | \bar{W}^1 | \bar{LB}^1 | \bar{UB}^1 | Mode | V_{DD} Current | DQL[7:0] ² | DQU[15:8] ² |
|-------------|-------------|-------------|--------------|--------------|------------------|--------------------|-----------------------|------------------------|
| H | X | X | X | X | Not selected | I_{SB1}, I_{SB2} | Hi-Z | Hi-Z |
| L | H | H | X | X | Output disabled | I_{DDR} | Hi-Z | Hi-Z |
| L | X | X | H | H | Output disabled | I_{DDR} | Hi-Z | Hi-Z |
| L | L | H | L | H | Lower Byte Read | I_{DDR} | D _{Out} | Hi-Z |
| L | L | H | H | L | Upper Byte Read | I_{DDR} | Hi-Z | D _{Out} |
| L | L | H | L | L | Word Read | I_{DDR} | D _{Out} | D _{Out} |
| L | X | L | L | H | Lower Byte Write | I_{DDW} | D _{in} | Hi-Z |
| L | X | L | H | L | Upper Byte Write | I_{DDW} | Hi-Z | D _{in} |
| L | X | L | L | L | Word Write | I_{DDW} | D _{in} | D _{in} |

¹ H = high, L = low, X = don't care

² Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings¹

| Symbol | Parameter | Conditions | Value | Unit |
|------------------|---|------------------------|------------------------|------|
| V_{DD} | Supply voltage ² | | -0.5 to 4.0 | V |
| V_{IN} | Voltage on an pin ² | | -0.5 to $V_{DD} + 0.5$ | V |
| I_{OUT} | Output current per pin | | ±20 | mA |
| P_D | Package power dissipation ³ | | 0.600 | W |
| T_{BIAS} | Temperature under bias | Commercial | -10 to 85 | °C |
| | | Industrial | -45 to 95 | °C |
| T_{stg} | Storage Temperature | | -55 to 150 | °C |
| T_{Lead} | Lead temperature during solder (3 minute max) | | 260 | °C |
| H_{max_write} | Maximum magnetic field | During Write | 8000 | A/m |
| H_{max_read} | Maximum magnetic field | During Read or Standby | | |

¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

² All voltages are referenced to V_{SS} . The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

³ Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

| Symbol | Parameter | Temp Range | Min | Typical | Max | Unit |
|----------|------------------------|------------|-------------------|---------|-----------------------------|------|
| V_{DD} | Power supply voltage | | 3.0 ¹ | 3.3 | 3.6 | V |
| V_{WI} | Write inhibit voltage | | 2.5 | 2.7 | 3.0 ¹ | V |
| V_{IH} | Input high voltage | | 2.2 | - | $V_{DD} + 0.3$ ² | V |
| V_{IL} | Input low voltage | | -0.5 ³ | - | 0.8 | V |
| T_A | Temperature under bias | Commercial | 0 | - | 70 | °C |
| | | Industrial | -40 | - | 85 | °C |

¹ There is a 2 ms startup time once V_{DD} exceeds $V_{DD}(\min)$. See **Power Up and Power Down Sequencing** below.

² $V_{IH}(\max) = V_{DD} + 0.3 V_{DC}$; $V_{IH}(\max) = V_{DD} + 2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

³ $V_{IL}(\min) = -0.5 V_{DC}$; $V_{IL}(\min) = -2.0 V_{AC}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(\min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The \bar{E} and \bar{W} control signals should track V_{DD} on power up to $V_{DD} - 0.2$ V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives \bar{E} and \bar{W} should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(\min)$.

Figure 2.1 Power Up and Power Down Diagram

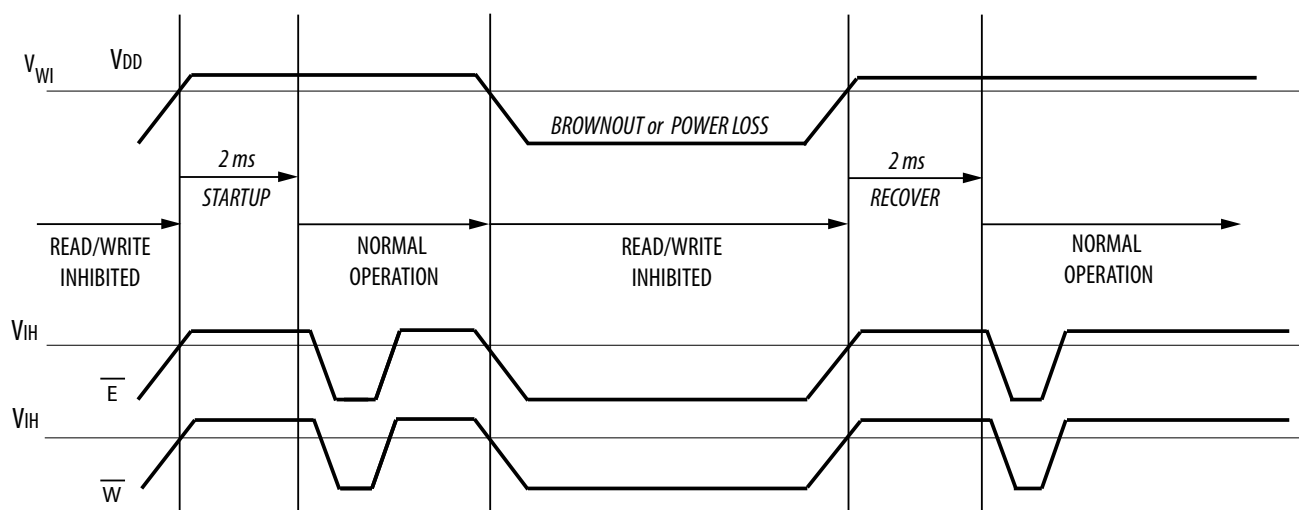


Table 2.3 DC Characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|------------------------|--------------------------|----------------|----------------|---------|
| $I_{lkg(I)}$ | Input leakage current | All | - | ± 1 | μA |
| $I_{lkg(O)}$ | Output leakage current | All | - | ± 1 | μA |
| V_{OL} | Output low voltage | $I_{OL} = +4 \text{ mA}$ | - | 0.4 | V |
| | | $I_{OL} = +100 \mu A$ | | $V_{SS} + 0.2$ | V |
| V_{OH} | Output high voltage | $I_{OH} = -4 \text{ mA}$ | 2.4 | - | V |
| | | $I_{OH} = -100 \mu A$ | $V_{DD} - 0.2$ | - | V |

Table 2.4 Power Supply Characteristics

| Symbol | Parameter | Typical | Max | Unit |
|-----------|--|---------|-----|------|
| I_{DDR} | AC active supply current - read modes ¹ ($I_{OUT} = 0 \text{ mA}$, $V_{DD} = \text{max}$) | 60 | 68 | mA |
| I_{DDW} | AC active supply current - write modes ¹ ($V_{DD} = \text{max}$) | 152 | 180 | mA |
| I_{SB1} | AC standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) <i>no other restrictions on other inputs</i> | 9 | 14 | mA |
| I_{SB2} | CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$) | 5 | 9 | mA |

¹ All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance ¹

| Symbol | Parameter | Typical | Max | Unit |
|-----------|---------------------------|---------|-----|------|
| C_{In} | Address input capacitance | - | 6 | pF |
| C_{In} | Control input capacitance | - | 6 | pF |
| $C_{I/O}$ | Input/Output capacitance | - | 8 | pF |

¹f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

| Parameter | Value | Unit |
|---|----------------|------|
| Logic input timing measurement reference level | 1.5 | V |
| Logic output timing measurement reference level | 1.5 | V |
| Logic input pulse levels | 0 or 3.0 | V |
| Input rise/fall time | 2 | ns |
| Output load for low and high impedance parameters | See Figure 3.1 | |
| Output load for all other timing parameters | See Figure 3.2 | |

Figure 3.1 Output Load Test Low and High



Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing ¹

| Symbol | Parameter | Min | Max | Unit |
|------------|---|-----|-----|------|
| t_{AVAV} | Read cycle time | 35 | - | ns |
| t_{AVQV} | Address access time | - | 35 | ns |
| t_{ELQV} | Enable access time ² | - | 35 | ns |
| t_{GLQV} | Output enable access time | - | 15 | ns |
| t_{BLQV} | Byte enable access time | - | 15 | ns |
| t_{AXQX} | Output hold from address change | 3 | - | ns |
| t_{ELQX} | Enable low to output active ³ | 3 | - | ns |
| t_{GLQX} | Output enable low to output active ³ | 0 | - | ns |
| t_{BLQX} | Byte enable low to output active ³ | 0 | - | ns |
| t_{EHQZ} | Enable high to output Hi-Z ³ | 0 | 15 | ns |
| t_{GHQZ} | Output enable high to output Hi-Z ³ | 0 | 10 | ns |
| t_{BHQZ} | Byte high to output Hi-Z ³ | 0 | 10 | ns |

¹ \bar{W} is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

² Addresses valid before or at the same time \bar{E} goes low.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

Figure 3.3B Read Cycle 2



Table 3.4 Write Cycle Timing 1 (\overline{W} Controlled) ¹

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVWL} | Address set-up time | 0 | - | ns |
| t_{AVWH} | Address valid to end of write (\overline{G} high) | 20 | - | ns |
| t_{AVWH} | Address valid to end of write (\overline{G} low) | 20 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (\overline{G} high) | 15 | - | ns |
| t_{WLWH} t_{WLEH} | Write pulse width (\overline{G} low) | 15 | - | ns |
| t_{DVWH} | Data valid to end of write | 10 | - | ns |
| t_{WHDX} | Data hold time | 0 | - | ns |
| t_{WLQZ} | Write low to data Hi-Z ³ | 0 | 15 | ns |
| t_{WHQX} | Write high to output active ³ | 3 | - | ns |
| t_{WHAX} | Write recovery time | 12 | - | ns |

¹ All write occurs during the overlap of \overline{E} low and \overline{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high impedance state. After \overline{W} , \overline{E} or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ This parameter is sampled and not 100% tested. Transition is measured ± 200 mV from the steady-state voltage. At any given voltage or temperature, $t_{WLQZ}(\text{max}) < t_{WHQX}(\text{min})$.

Figure 3.4 Write Cycle Timing 1 (\overline{W} Controlled)



Table 3.5 Write Cycle Timing 2 (\bar{E} Controlled) ¹

| Symbol | Parameter | Min | Max | Unit |
|--------------------------|--|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVEL} | Address set-up time | 0 | - | ns |
| t_{AVEH} | Address valid to end of write (\bar{G} high) | 20 | - | ns |
| t_{AVEH} | Address valid to end of write (\bar{G} low) | 20 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (\bar{G} high) | 15 | - | ns |
| t_{ELEH} t_{ELWH} | Enable to end of write (\bar{G} low) ³ | 15 | - | ns |
| t_{DVEH} | Data valid to end of write | 10 | - | ns |
| t_{EHDX} | Data hold time | 0 | - | ns |
| t_{EHAX} | Write recovery time | 12 | - | ns |

¹ All write occurs during the overlap of \bar{E} low and \bar{W} low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If \bar{G} goes low at the same time or after \bar{W} goes low, the output will remain in a high impedance state. After \bar{W} , \bar{E} or \bar{UB}/\bar{LB} has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between \bar{E} being asserted low in one cycle to \bar{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.

³ If \bar{E} goes low at the same time or after \bar{W} goes low, the output will remain in a high-impedance state. If \bar{E} goes high at the same time or before \bar{W} goes high, the output will remain in a high-impedance state.

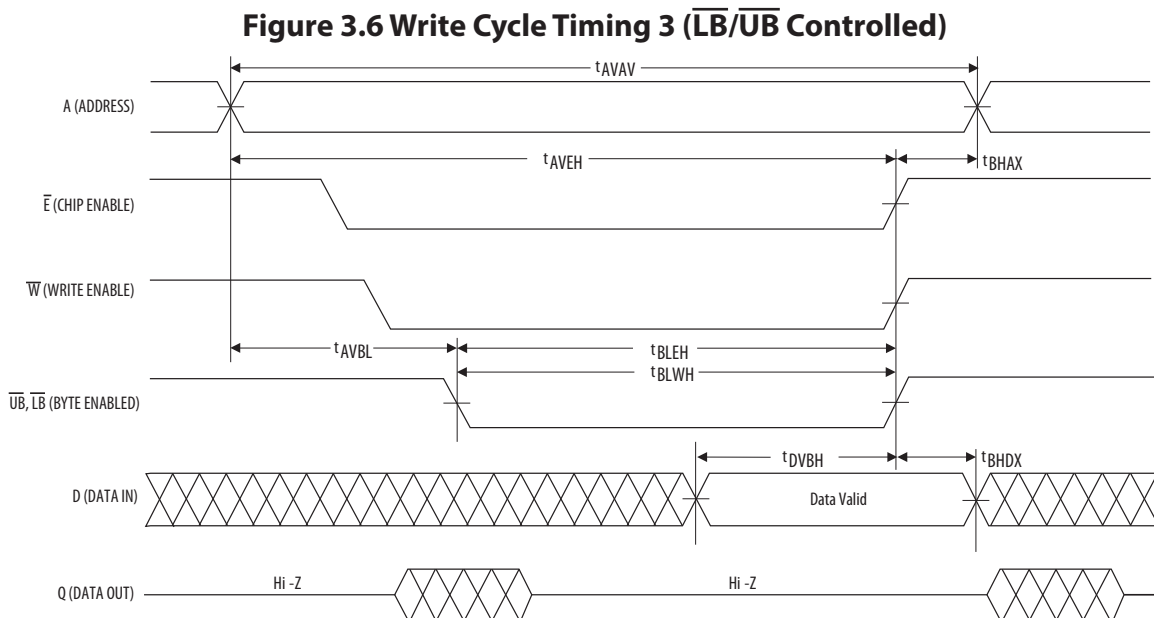
Figure 3.5 Write Cycle Timing 2 (\bar{E} Controlled)

Table 3.6 Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled) ¹

| Symbol | Parameter | Min | Max | Unit |
|--|---|-----|-----|------|
| t_{AVAV} | Write cycle time ² | 35 | - | ns |
| t_{AVBL} | Address set-up time | 0 | - | ns |
| t_{AVBH} | Address valid to end of write ($\overline{\text{G}}$ high) | 20 | - | ns |
| t_{AVBH} | Address valid to end of write ($\overline{\text{G}}$ low) | 20 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width ($\overline{\text{G}}$ high) | 15 | - | ns |
| t_{BLEH} t_{BLWH} | Write pulse width ($\overline{\text{G}}$ low) | 15 | - | ns |
| t_{DVBH} | Data valid to end of write | 10 | - | ns |
| t_{BHDX} | Data hold time | 0 | - | ns |
| t_{BHAX} | Write recovery time | 12 | - | ns |

¹ All write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high impedance state. After $\overline{\text{W}}$, $\overline{\text{E}}$ or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

² All write cycle timings are referenced from the last valid address to the first transition address.



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

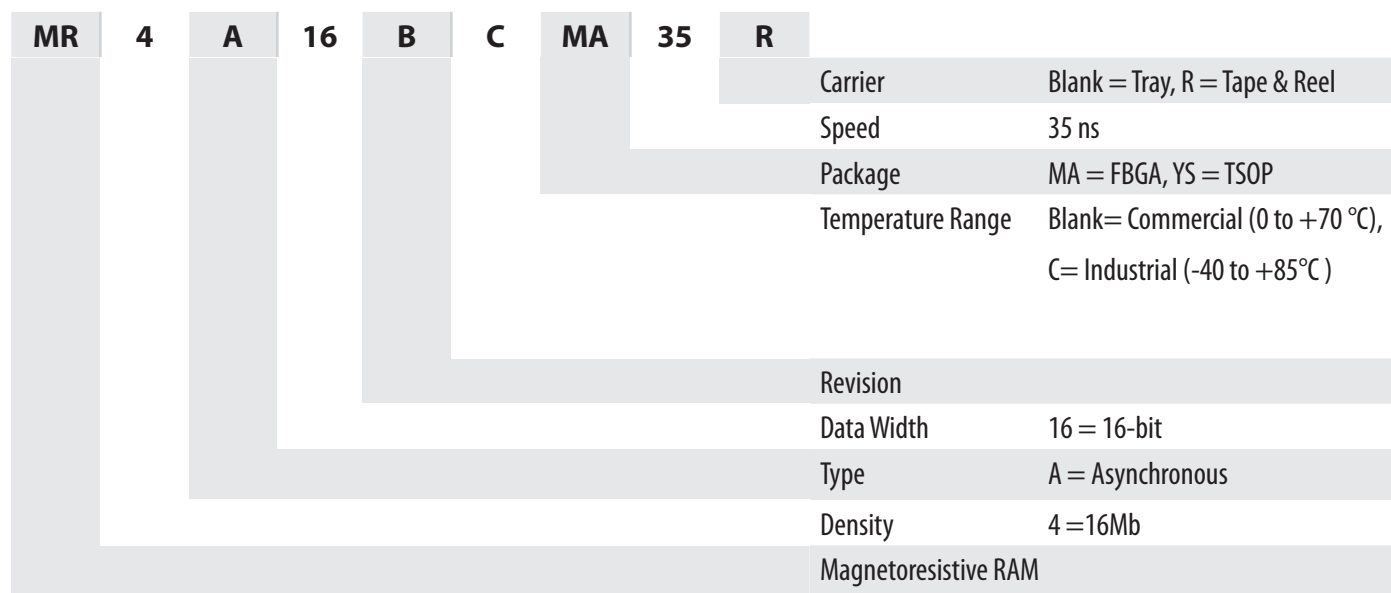


Table 4.1 Available Parts

| Grade | Temp Range | Package | Shipping Container | Order Part Number |
|------------|--------------|----------|--------------------|-------------------|
| Commercial | 0 to +70 °C | 48-BGA | Trays | MR4A16BMA35 |
| | | | Tape & Reel | MR4A16BMA35R |
| | | 54-TSOP2 | Trays | MR4A16BYS35 |
| | | | Tape & Reel | MR4A16BYS35R |
| Industrial | -40 to +85°C | 48-BGA | Tray | MR4A16BCMA35 |
| | | | Tape & Reel | MR4A16BCMA35R |
| | | 54-TSOP2 | Tray | MR4A16BCYS35 |
| | | | Tape & Reel | MR4A16BCYS35R |

5. MECHANICAL DRAWING

Figure 5.1 48-FBGA

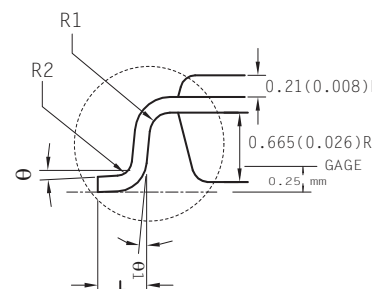


Print Version Not To Scale

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
- ③ 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- ④ Dimension 'ddd' is measured parallel to primary datum C.
- ⑤ Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

5. MECHANICAL DRAWING

Figure 5.2 54-TSOP2



| Ref | Min | Nominal | Max |
|-----|----------|---------|-------|
| A | | | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.30 | 0.35 | 0.45 |
| c | 0.12 | | 0.21 |
| D | 22.10 | 22.22 | 22.35 |
| E | 11.56 | 11.76 | 11.95 |
| E1 | 10.03 | 10.16 | 10.29 |
| e | 0.80 BSC | | |
| L | 0.40 | 0.50 | 0.60 |
| L1 | 0.80 REF | | |
| R1 | 0.12 | - | - |
| R2 | 0.12 | - | 0.25 |
| θ | 0° | - | 8° |
| θ1 | 0.40 | - | - |
| θ2 | 15° REF | | |
| θ3 | 15° REF | | |

Print Version Not To Scale

1. Dimensions in Millimeters.
2. Package dimensions refer to JEDEC MS-024



6. REVISION HISTORY

| Rev | Date | Description of Change |
|------|--------------------|--|
| 1 | May 29, 2009 | Establish Speed and Power Specifications |
| 2 | July 27, 2009 | Increase BGA Package to 11 mm x 11 mm |
| 3 | Nov 26, 2009 | Changed ball definition of H6 to A19 and G2 to NC in Figure 1.2. |
| 4 | Mar 10, 2010 | Changed speed marking and timing specs to 35 ns part. Changed BGA package to 10 mm x 10mm |
| 5 | Apr 7, 2010 | Added 54-TSOP package options. |
| 6 | Oct 7, 2011 | Added AEC-Q100 Grade 1 product option. Max. magnetic field during write (H_{max_write}) increased to 8000 A/m. Revised IDDW typical from 110 to 152mA, max from TBD to 180mA; IDDR max from TBD to 68mA; ISB1 typical from 11 to 9mA; ISB2 from typical 7 to 5mA. |
| 7 | Oct 28, 2011 | Added note to BGA package option products are MSL-6 only, MSL-3 qualification underway. Fixed typo on BGA drawing: Top View incorrectly labeled Bottom View. |
| 8 | August 6, 2012 | Figure 2.1 Power Up and Power Down Timing redrawn. Added 54-TSOP illustrations. Reformatted all parametric tables. Reformatted Table 4.1 Ordering Part Numbers. |
| 9 | August 27, 2013 | Corrected the AEC Q-100 Grade A ordering option to be available in 54-TSOP2, not 48-BGA. |
| 9.1 | January 29, 2014 | Corrected minor typo in Ordering PN table. |
| 10 | April 25, 2014 | AEC-Q100 removed until qualified product is available. |
| 11 | September 17, 2014 | 48-BGA package options moisture sensitivity level upgraded to MSL-5. |
| 11.1 | May 19, 2015 | Revised Everspin contact information. |
| 11.2 | June 11, 2015 | Corrected Japan Sales Office telephone number. |
| 11.3 | July 29, 2015 | Minor correction to the 'ddd' tolerance value for the BGA Package (Note 4.) |
| 11.4 | March 11, 2016 | The BGA package moisture sensitivity level rating is changed to MSL-6 in Table 4.1. |
| 11.5 | November 22, 2016 | The BGA package moisture sensitivity level rating is changed to MSL-5 in Table 4.1. |
| 11.6 | May 09, 2017 | All products meet MSL-3 moisture sensitivity level |
| 11.7 | March 23, 2018 | Updated the Contact Us table |

7. HOW TO CONTACT US

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Filename:

EST00352_MR4A16B_Datasheet_Rev11.7032318

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