

# aPR33A3

## Tape Mode (C3.1)

# Datasheet

## Recording voice IC

### APLUS INTEGRATED CIRCUITS INC.

**Address:**

3 F-10, No. 32, Sec. 1, Chenggung Rd., Taipei, Taiwan 115, R.O.C.

**TEL:**

886-2-2782-9266

**FAX:**

886-2-2782-9255

**WEBSITE :**

<http://www.aplusinc.com.tw>

**Technology E-mail:**

[service@aplusinc.com.tw](mailto:service@aplusinc.com.tw)

**Sales E-mail:**

[sales@aplusinc.com.tw](mailto:sales@aplusinc.com.tw)

**■ FEATURES**

- Operating Voltage Range: 3V ~ 6.5V
- Single Chip, High Quality Audio/Voice Recording & Playback Solution
  - ◆ No External ICs Required
  - ◆ Minimum External Components
- User Friendly, Easy to Use Operation
  - ◆ Programming & Development Systems Not Required
- 680 sec. Voice Recording Length in aPR33A3
- Powerful 16-Bits Digital Audio Processor.
- Nonvolatile Flash Memory Technology
  - ◆ No Battery Backup Required
- External Reset pin.
- Powerful Power Management Unit
  - ◆ Very Low Standby Current: 1uA
  - ◆ Low Power-Down Current: 15uA
  - ◆ Supports Power-Down Mode for Power Saving
- Built-in Audio-Recording Microphone Amplifier
  - ◆ No External OPAMP or BJT Required
  - ◆ Easy to PCB layout
- Configurable analog interface
  - ◆ Differential-ended MIC pre-amp for Low Noise
  - ◆ High Quality Line Receiver
- High Quality Analog to Digital, DAC and PWM module
  - ◆ Resolution up to 16-bits
- Simple And Direct User Interface
- Tape mode manages messages

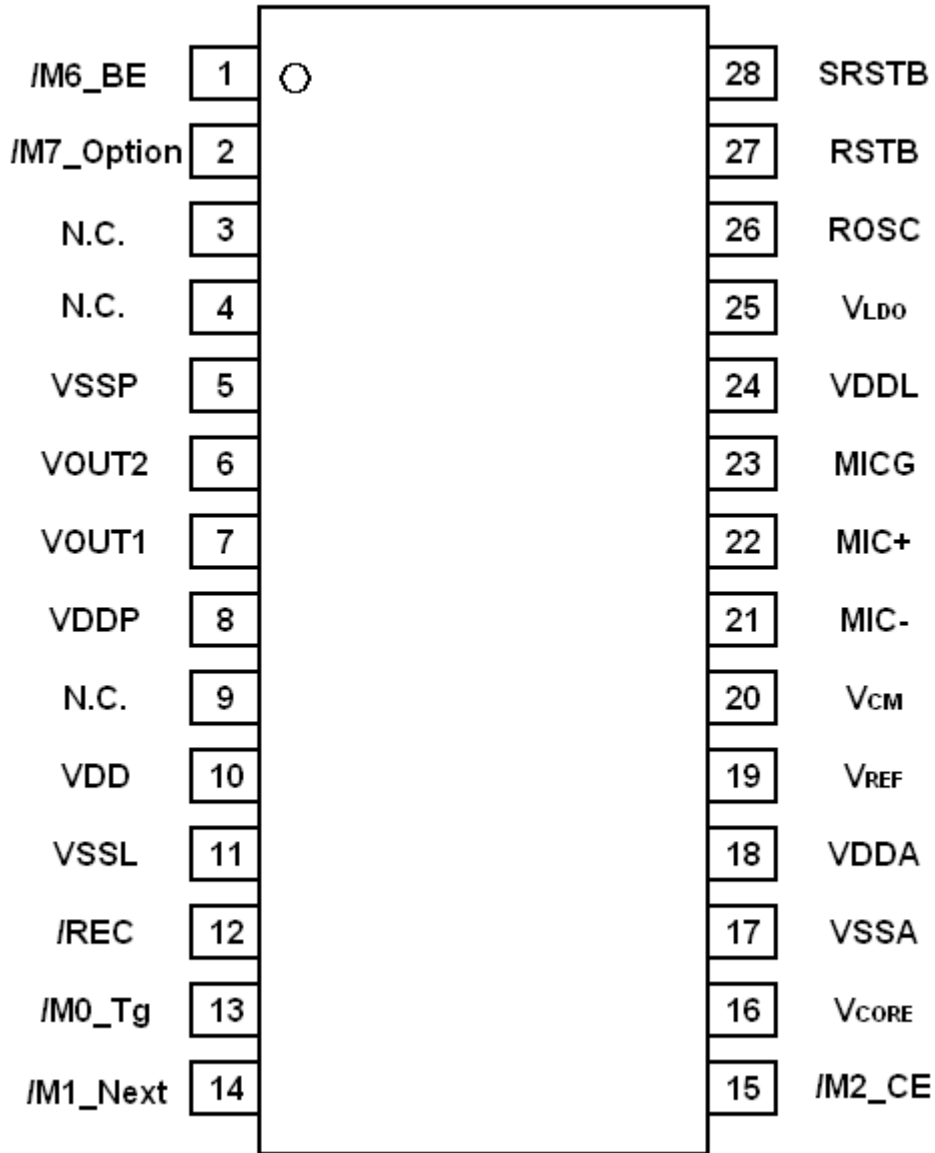
## ■ DESCRIPTION

Today's consumers demand the best in audio/voice. They want crystal-clear sound wherever they are in whatever format they want to use. APLUS delivers the technology to enhance a listener's audio/voice experience.

The aPR33A series are powerful audio processor along with high performance audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The aPR33A series are a fully integrated solution offering high performance and unparalleled integration with analog input, digital processing and analog output functionality. The aPR33A series incorporates all the functionality required to perform demanding audio/voice applications. High quality audio/voice systems with lower bill-of-material costs can be implemented with the aPR33A series because of its integrated analog data converters and full suite of quality-enhancing features such as sample-rate convertor.

The aPR33A series C3.1 is Tape mode manages messages sequentially much like traditional cassette tape recorders. Within tape mode two options exist, auto rewind and non-auto rewind. Auto rewind mode configures the device to automatically rewind to the beginning of the message immediately following recording or playback of the message. In tape mode, using either option, messages must be recorded or played back sequentially, much like a traditional cassette tape recorder specially designed for simple key trigger, user can record and playback the message. Meanwhile, this mode provides the power-management system. Users can let the chip enter power-down mode when unused. It can effectively reduce electric current consuming to 15uA and increase the using time in any projects powered by batteries.

■ PIN CONFIGURATION

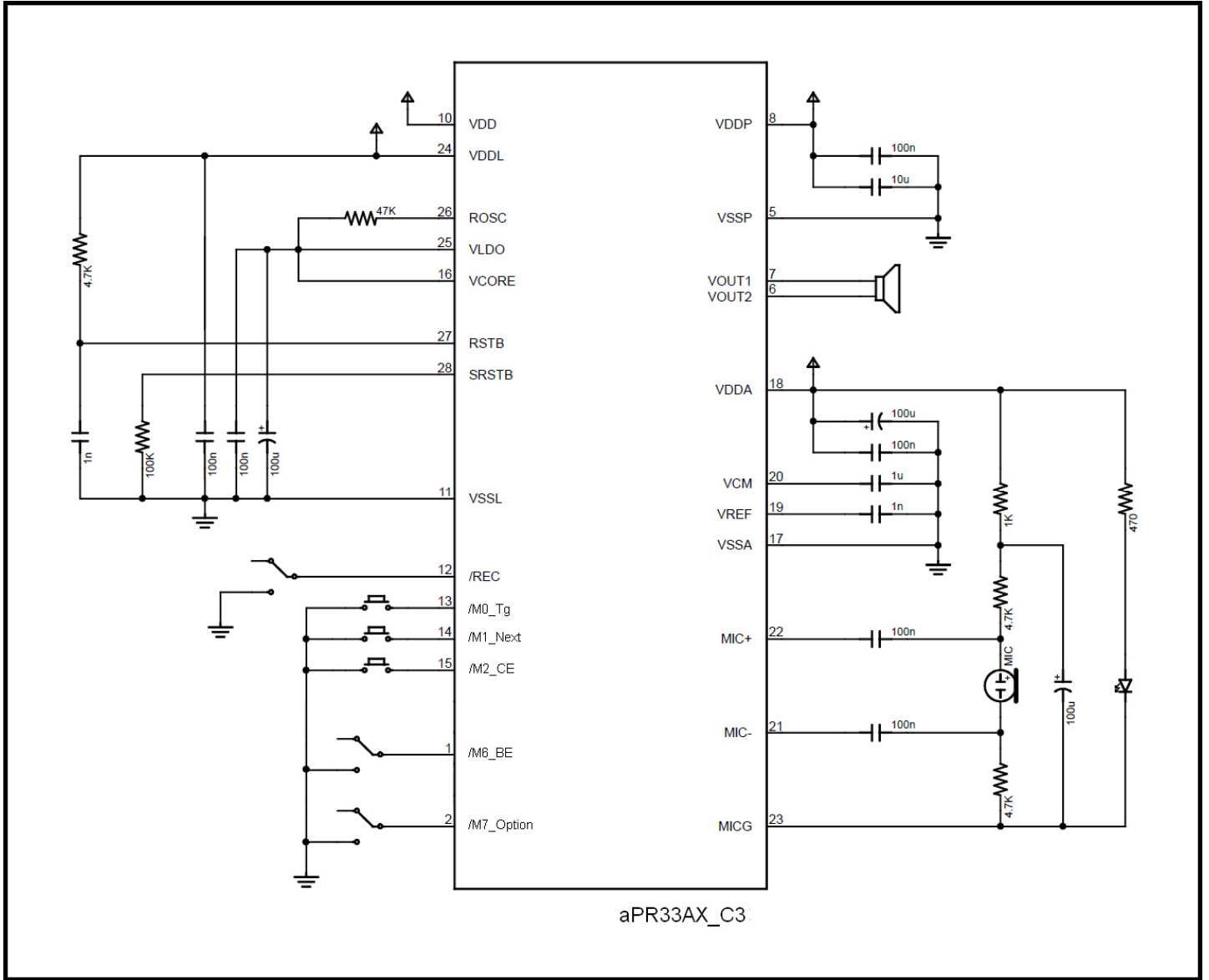


DIP / SOP Package

**■ PIN DESCRIPTION**

Pin Names	Pin No	TYPE	Description
VDDP	8		Positive power supply.
VDD	10		
VDDA	18		
VDDL	24		
VSSP	5		Power ground.
VSSL	11		
VSSA	17		
VLDO	25		Internal LDO output.
V <sub>CORE</sub>	16		Positive power supply for core.
V <sub>REF</sub>	19		Reference voltage.
V <sub>CM</sub>	20		Common mode voltage.
Rosc	26	INPUT	Oscillator resistor input.
/RSTB	27	INPUT	Reset. (Low active)
SRSTB	28	INPUT	System reset, pull-down a resistor to the VSSL.
MIC+	21	INPUT	Microphone differential input.
MIC-	22		
MICG	23	OUTPUT	Microphone ground.
VOUT1	7	INPUT	PWM output to drive speaker directly. DAC option.
VOUT2	6	INPUT	PWM output to drive speaker directly. DAC output.
/REC	12	INPUT	Record Mode. (Low active)
/M0_Tg	13	INPUT	Play/Record trigger. (Low active)
/M1_Next	14	INPUT	This pin forces a jump to next message for either recording or playback. (Low active)
/M2_/CE	15	INPUT	Reset message management features. (Low active)
/M6_BE	1	INPUT	Beep enable/disable. (Low active)
/M7_Option	2	INPUT	Auto Rewind / Non-Auto Rewind (Low active) mode select.

■ TYPICAL APPLICATION

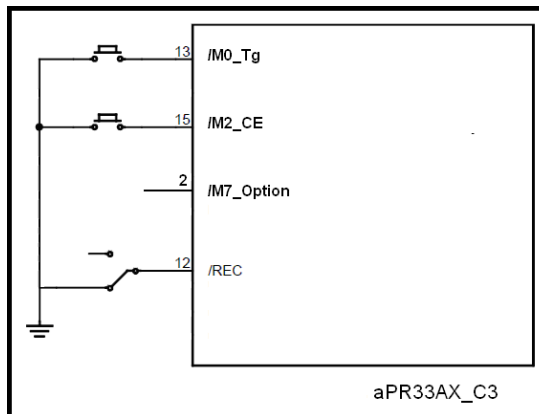


■ **MESSAGE MODE**

In tape message mode (C3.1), users can divide the memory sequentially much like traditional cassette tape recorders. Within tape mode, there are two options - auto rewind and non-auto rewind which will be applied by the /M7\_Option pin.

- Tape Mode using the Auto Rewind Option of record

The following fig. showed a typical record circuit for auto rewind mode. We add a slide-switch between /REC pin and VSS, and add 2 tact-switches /M0\_Tg, /M2\_CE pin and VSS. When the slide-switch fixed in VSS side and press /M0\_TG tact switch, chip will start message record and until the users release the tact-switch.

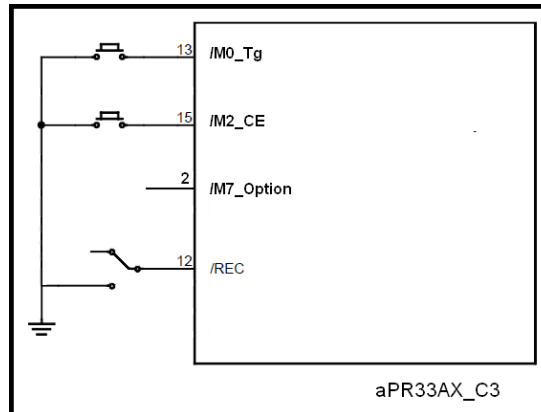


Note: After reset, /REC and /M0\_Tg, /M2\_/CE and /M7\_Option pin will be pull-up to VDD by internal resistor.

On power-up, the device is ready to record or playback from the first address of the memory array. Send a falling edge to the /M0\_Tg pin the device will beep once and start recording. A subsequent rising edge to the /M0\_Tg pin will stop recording & beep once. If the M0\_Tg pin is kept in low potential to the end of the memory, the recording will stop automatically & beep once regardless of the state of the /M0\_Tg pin. The device returns to the standby mode and the /M0\_Tg pin is returned to high. Please note the next recording operation will totally cover all your previous messages. Your new recorded message will be your first message and your original messages will be lost.

- Tape Mode using the Auto Rewind Option of playback

The following fig. showed a typical playback circuit for auto rewind mode. We add a slide-switch between /REC pin and VSS, and add 2 tact-switches /M0\_Tg, /M2\_CE pin and VSS. When the slide-switch fixed in float side and press /M0\_Tg pin, chip will start message playback.



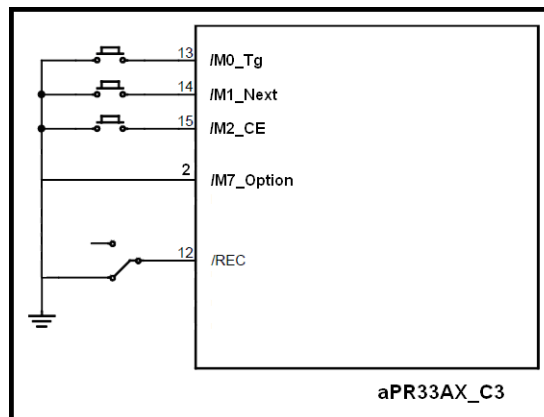
Note: After reset, /REC and /M0\_Tg, /M2\_/CE and /M7\_Option pin will be pull-up to VDD by internal resistor.

On power-up, beep twice and the device will be ready to playback from the first address of memory array. Send a falling edge to the /M0\_Tg pin to play the present message. During the playback, send a falling edge to /M0\_Tg pin then it will stop playing & beep once. After stop playing, sending a falling edge to /M0\_Tg pin again, it will start to play the next message. After playing the last message, send a falling edge to /M0\_Tg pin, and it will beep once to remind you & auto-rewind to the first message. If /M0\_Tg pin is kept in low potential continually, the messages will be played to the last one & beep twice repeatedly. When /M0\_Tg pin is back to high potential, the beep voices stop and the message will be auto-rewind to the first message.



- Tape Mode using the Non-Auto Rewind Option of record

The following fig. showed a typical record circuit for non-auto rewind mode. We add a slide-switch between /REC pin and VSS, and add 3 tact-switches /M0\_Tg, /M1\_Next, /M2\_CE pin and VSS. When the slide-switch fixed in Vss side and press /M0\_Tg tact-switch , chip will start message record and until the users release the tact-switch. If you want to record a new message, please press /M1\_Next switch to go to the next section.



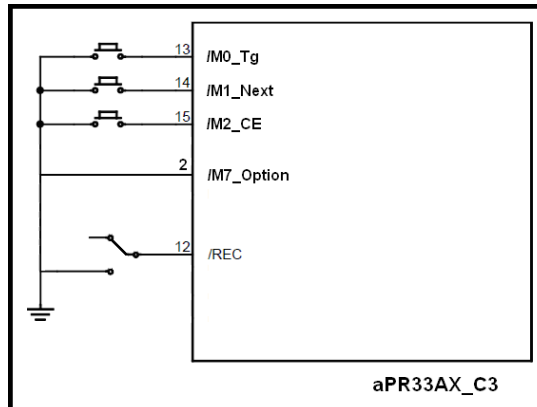
Note: After reset, /REC and /M0\_Tg, /M1\_Next, /M2\_/CE and /M7\_Option pin will be pull-up to VDD by internal resistor.

On power-up, beep twice and the device is ready to record from the first address of memory array. Send a falling edge to /M0\_Tg pin and it will start recording & beep once. It must be kept in low potential when recording. Send a rising edge to /M0\_Tg pin and it will stop recording & beep once. If /M0\_Tg is kept in low potential and over the acceptable memory, it will stop recording automatically & beep once. When /M0\_Tg pin is rising in high potential, the device will auto-rewind to the beginning place of the message & keep in standby mode to wait for a new command. Please note the next recording operation will cover your original message so the users have to send a falling edge to /M1\_Next pin to let the device goes to the next message to protect your original data.

This mode allows the users easily record a new message to cover the original message unnecessarily triggering /M1\_Tg pin. If you need to cover the other messages, send a falling edge to /M2\_CE pin to back to the beginning of the memory then send falling edges to /M1\_Next pin to the message that you want to be covered. When you cover this message, it will be the last message. The original ones behind this message will be totally lost.

- Tape Mode using the Non-Auto Rewind Option of playback

The following fig. showed a typical playback circuit for non-auto rewind mode. We add a slide-switch between /REC pin and VSS, and add 3 tact-switches /M0\_Tg, /M1\_Next, /M2\_CE pin and VSS. When the slide-switch fixed in float side and press /M0\_Tg tact-switch , chip will start message playback.



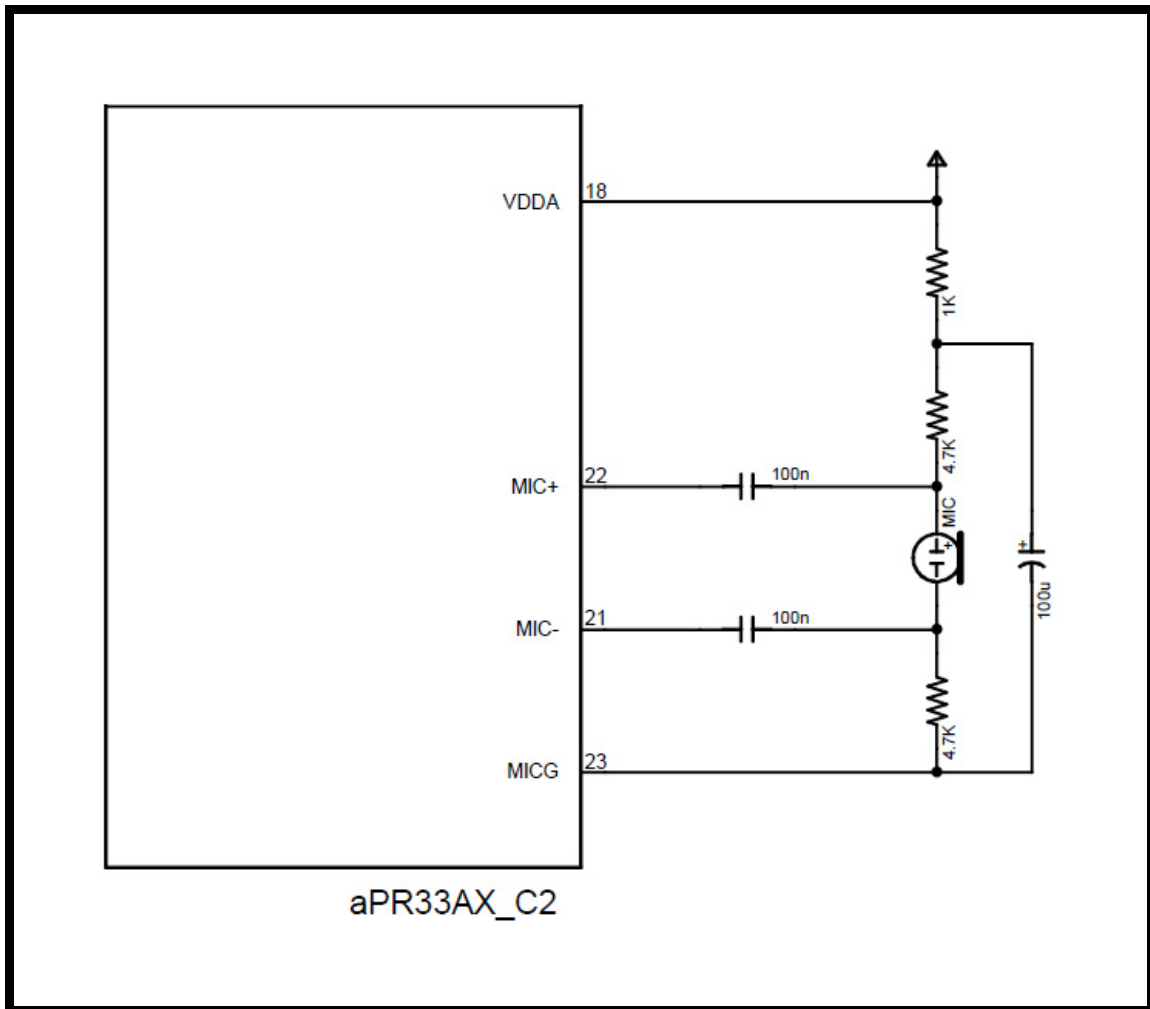
Note: After reset, /REC and /M0\_Tg, /M1\_Next, /M2\_/CE and /M7\_Option pin will be pull-up to VDD by internal resistor.

On power-up, beep twice and the device will be ready to play from the first address of memory array. Send a falling edge to /M0\_Tg pin then it will play from the first message & beep once. During the playback, if /M0\_Tg pin receive the falling edge then it will stop playback immediately. After stop playing, send a falling edge to /M0\_Tg pin and it will play the message from the beginning. If you keep /M0\_Tg pin in low potential, this message will loop playing. Send a falling edge to /M2\_CE pin, beep once & go back to the first message to wait for the next command.

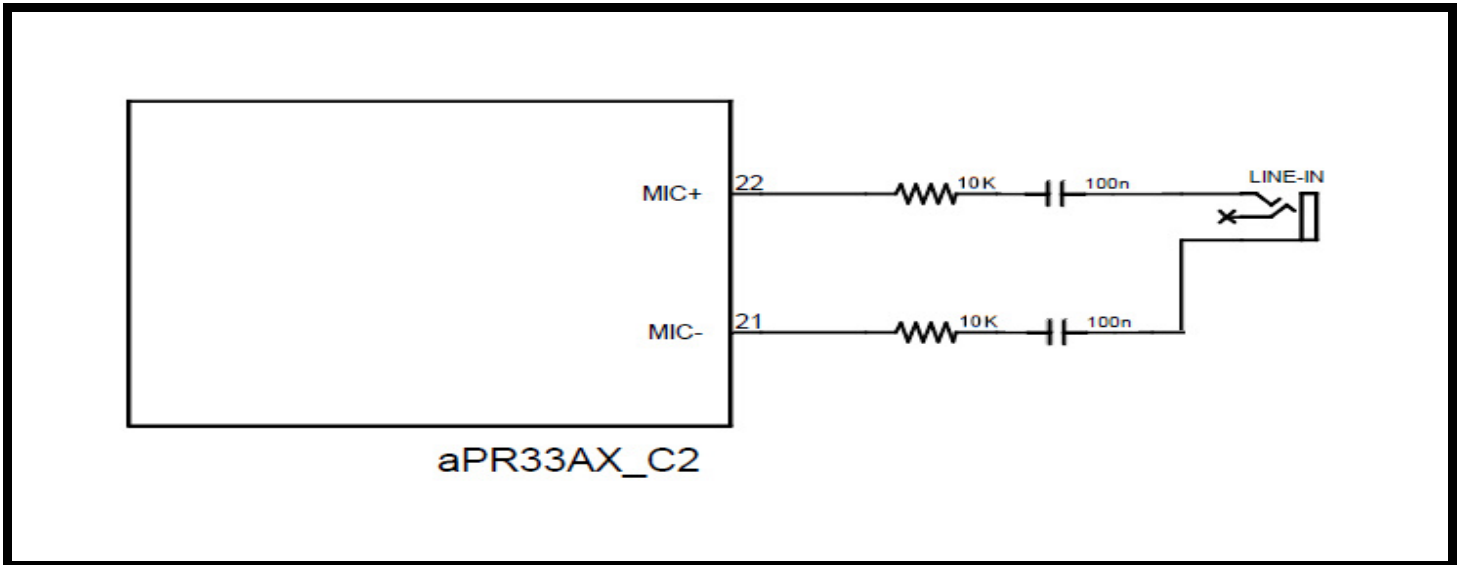
Please note the mode only can play the present message. If you want to hear the next message, you have to send a falling edge to /M1\_Next pin to complete ( beep once ). When arrive to the end of memory, sending a falling edge to /M0\_Tg pin again, the device will beep twice and go back to the first message to wait for a new command.

■ **VOICE INPUT**

The aPR33A series supported single channel voice input by microphone or line-in. The following fig. showed circuit for different input methods: microphone, line-in and mixture of both.

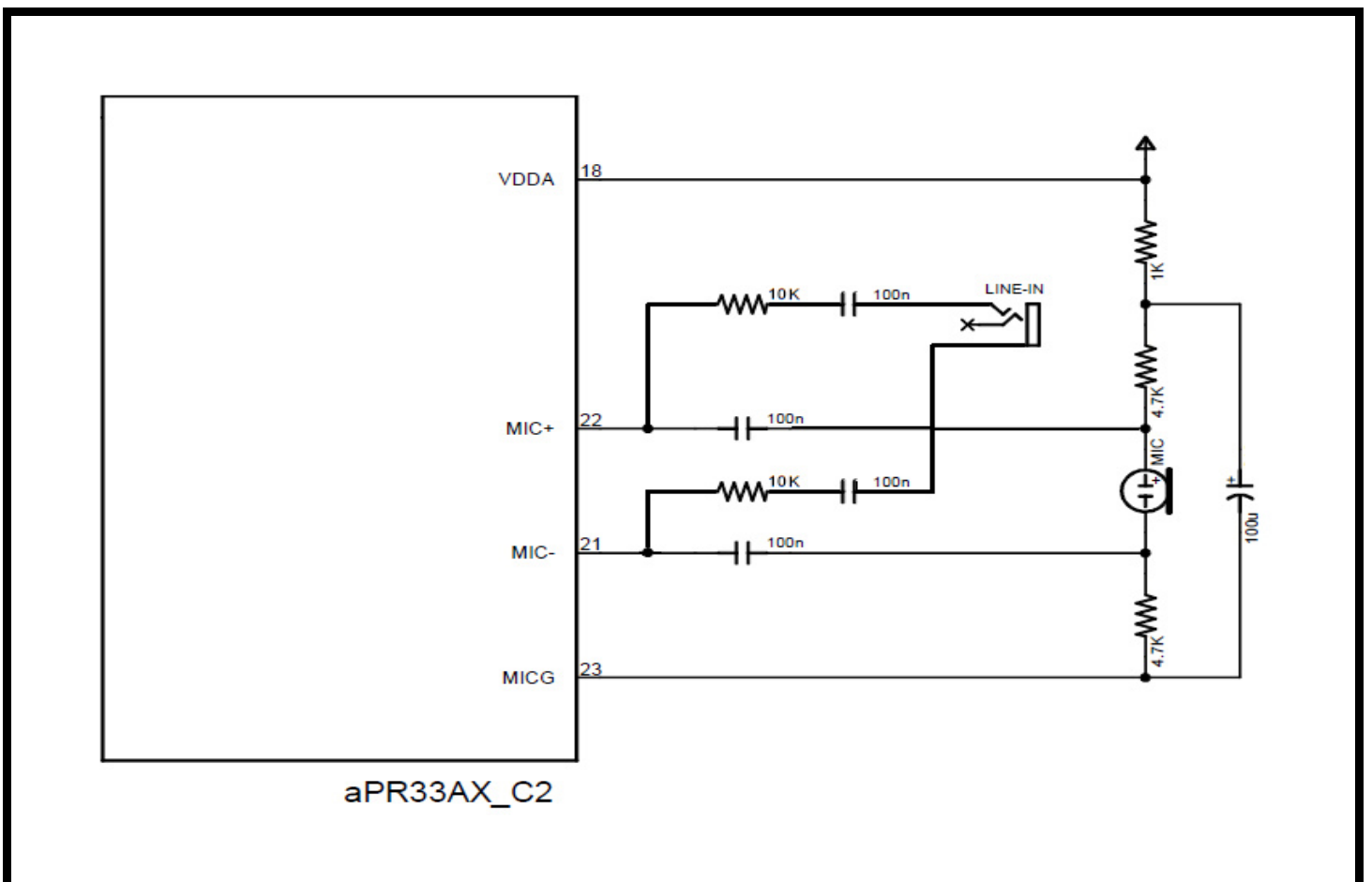


(A) Microphone



Note: The 10K resistor used for input signal adjust, and the value just for reference.

**(B) Line-In**



Note: The 10K resistor used for input signal adjust, and the value just for reference.

**(C) Microphone + Line-In**

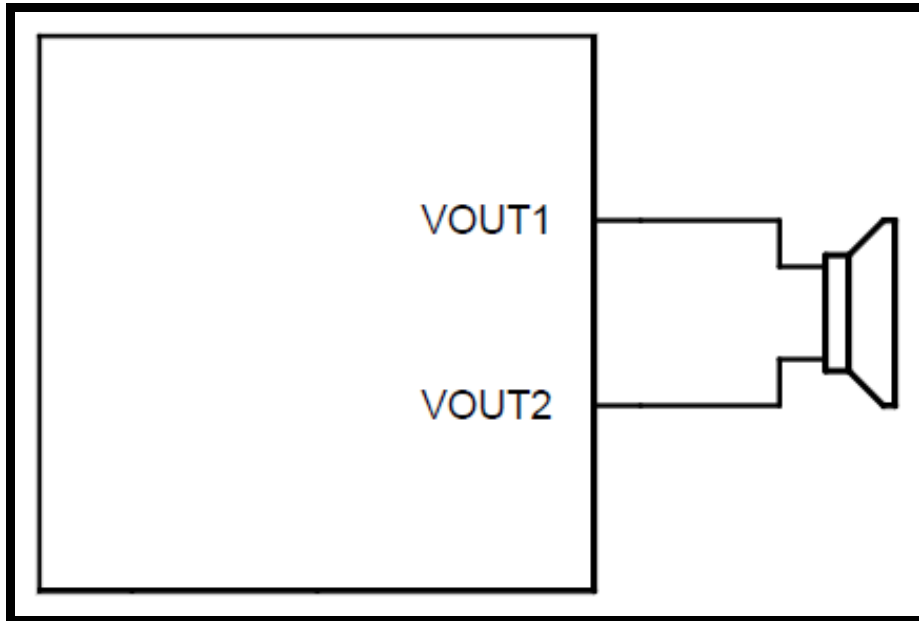
■ **VOICE OUTPUT**

The aPR33A series support 2 voice output mode, PWM and DAC.

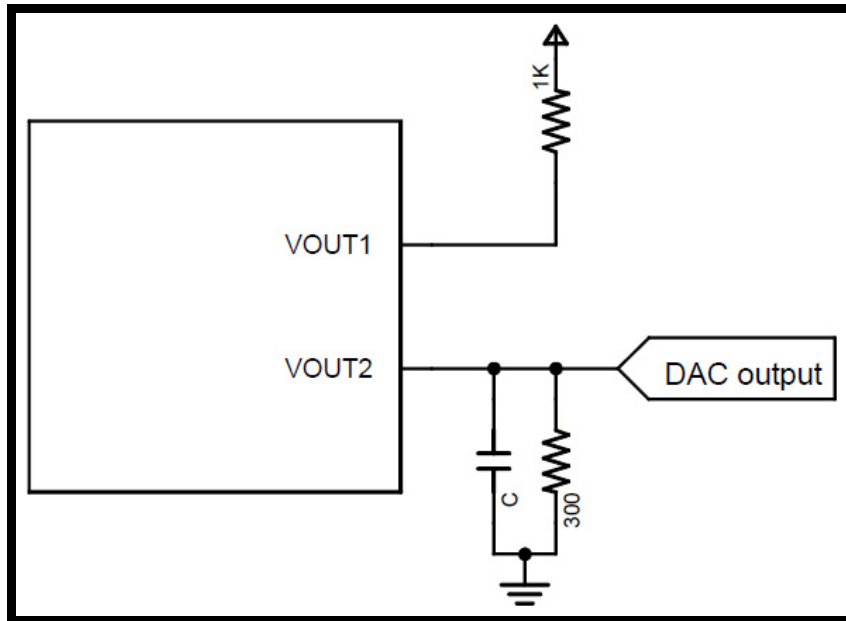
The PWM mode use VOUT1 and VOUT2 pin to drive speaker directly without external components to save cost.

The DAC mode use VOUT2 pin to output current signal. User can use the signal to drive audio amplifier or mix with other components in their applications to provide larger voice volume.

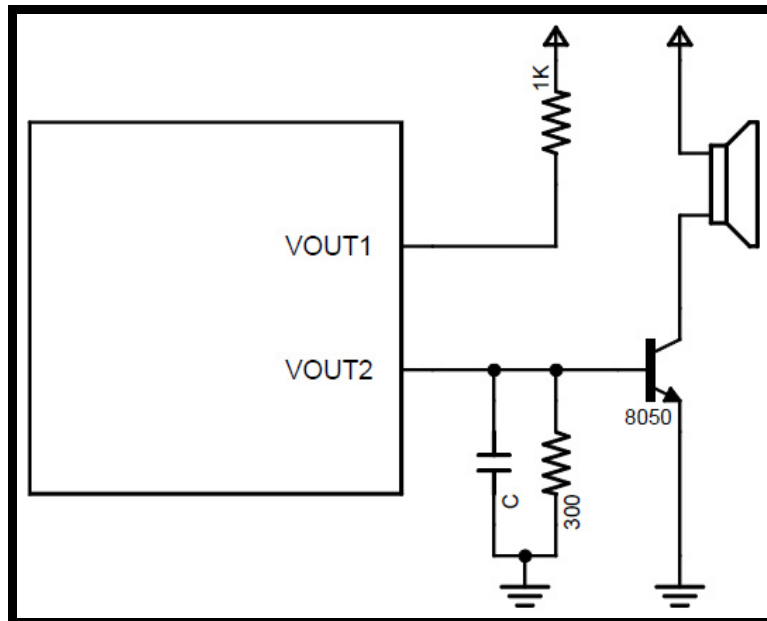
The following fig. show circuit for different output methods: PWM, DAC, DAC with transistor, DAC with audio amplifier AP4890B.



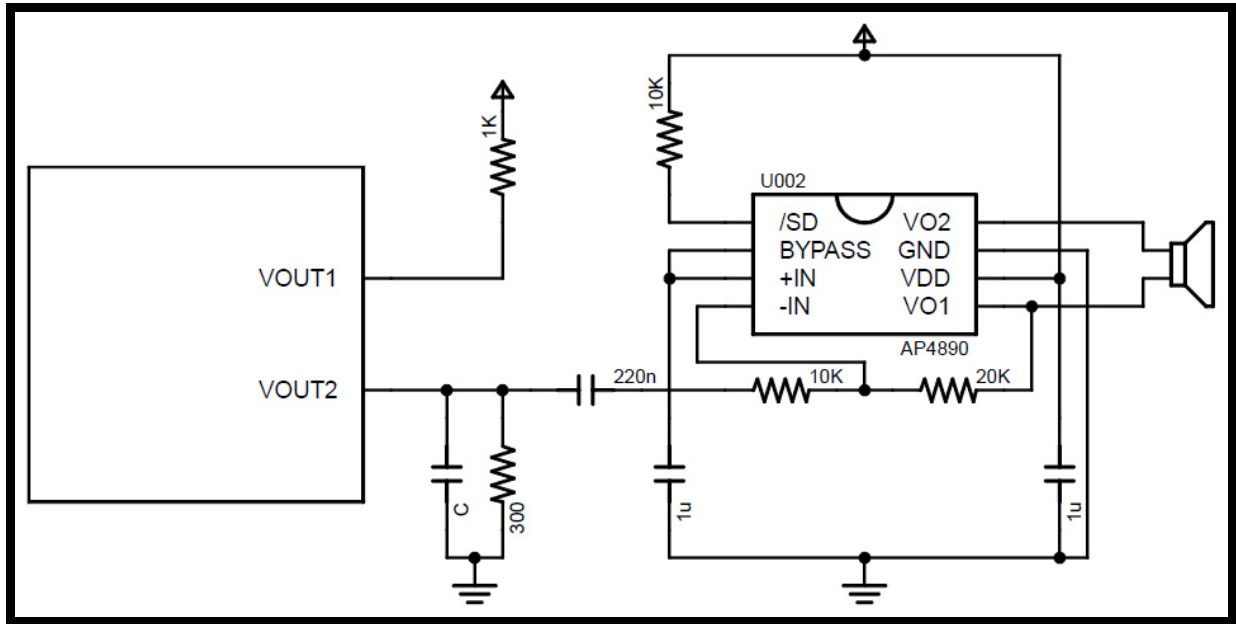
(A) PWM



(B) DAC



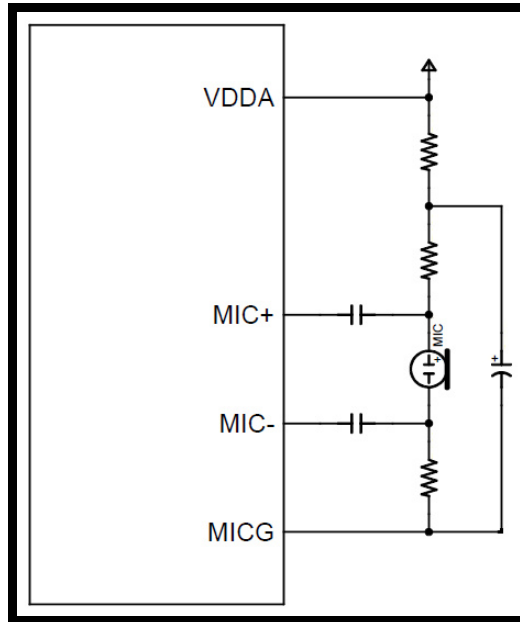
(C) DAC with transistor



**(D) DAC with audio amplifier AP4890B**

■ **BUSY**

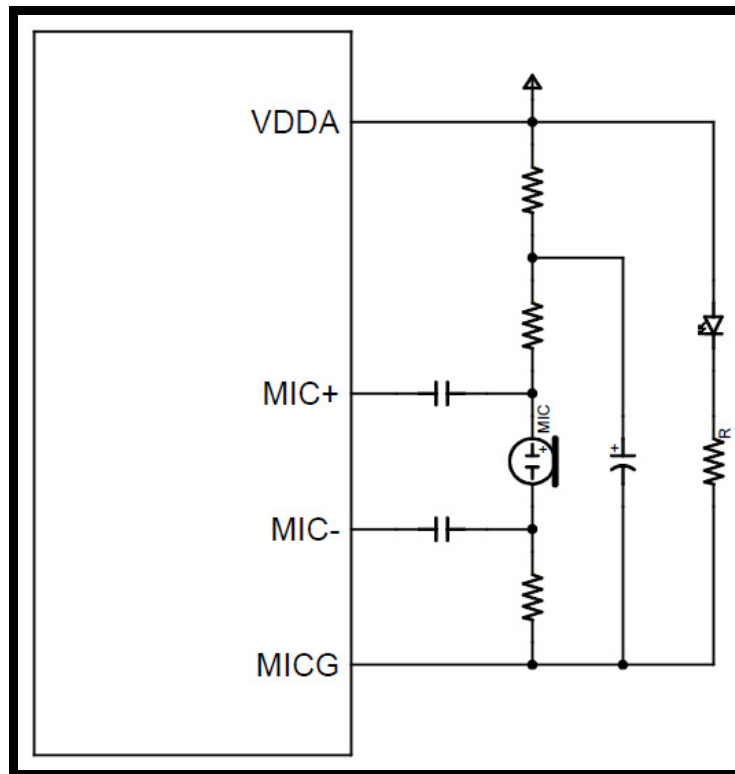
The MICG pin will be drove to low during the message record or playback, and drove to high during idle or standby, user can detect MICG status to know chip is busy or not.



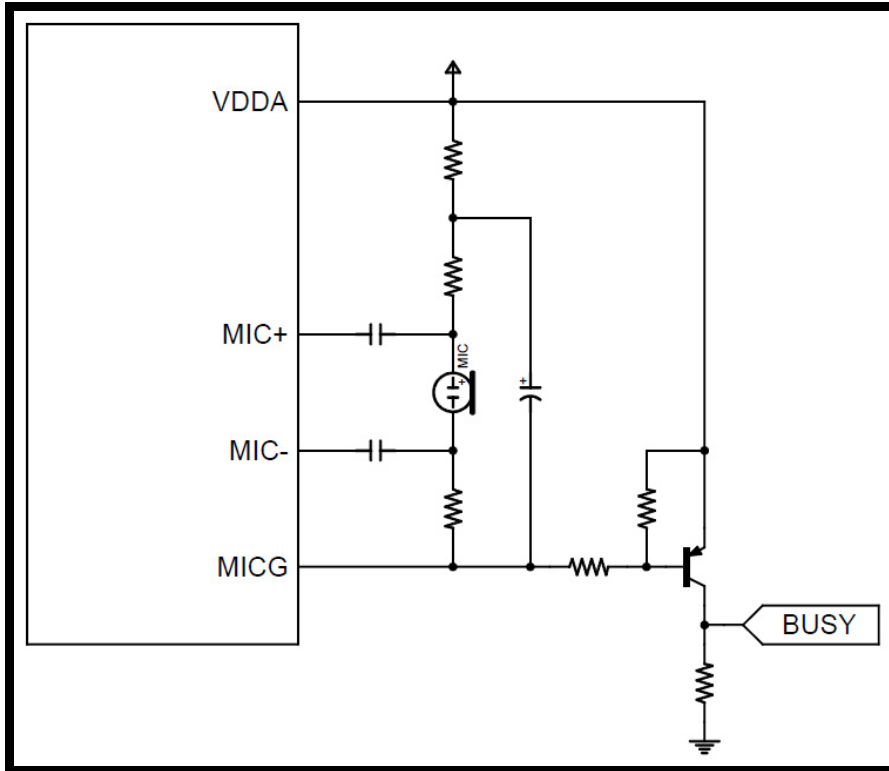
Please note it is limited for MICG pin driving current. Reference to  $I_{OH}$  and  $I_{OL}$  in section “**DC CHARACTERISTICS**”. If MICG pin is over loading from external circuit, it will cause noise in microphone circuit.



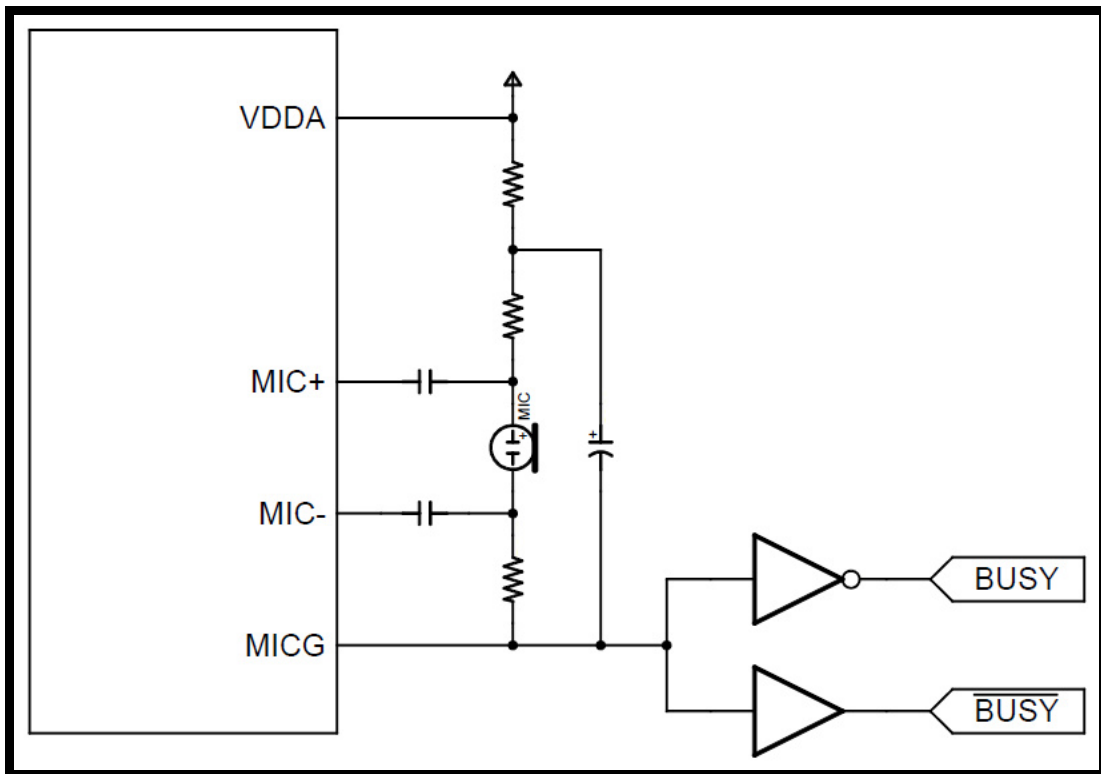
Below is a typical application. We add one LED to indicate IC record and playback status. We use one Resistor to limit current. And suggest  $R > 470\Omega$



Below Transistor circuit is to get higher current, larger than  $I_{OH}$  or  $I_{OL}$ .



To get best sound quality, we can use buffer or inverter to isolate MICG to avoid noise from external circuit. Driving current is provided by buffer(inverter) only.

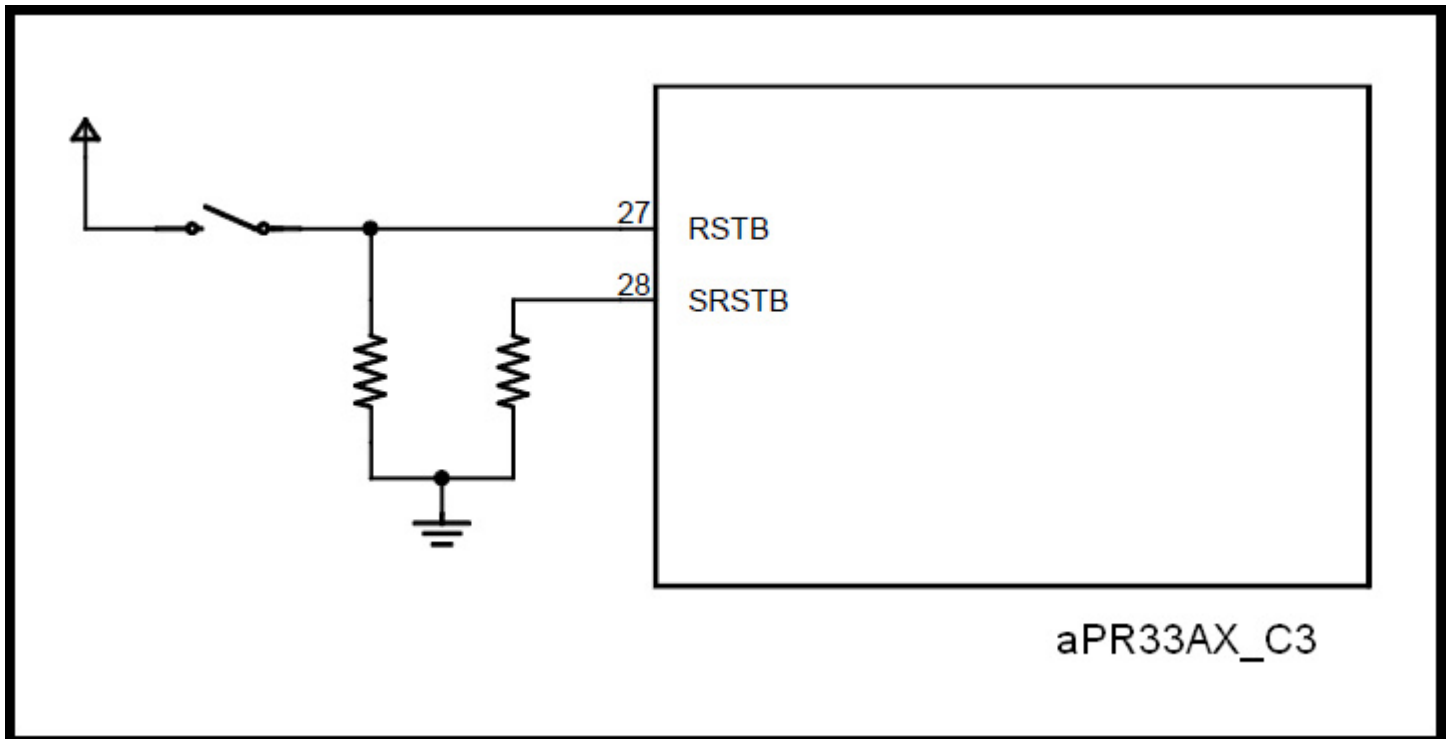


■ **RESET**

aPR33AX series can enter standby mode when RSTB pin drive to low. During chip in the standby mode, the current consumption is reduced to  $I_{SB}$  and any operation will be stopped, user also can not execute any new operate in this mode.

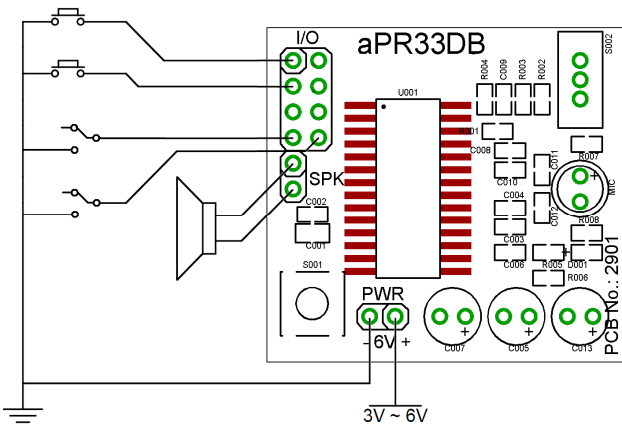
The standby mode will continue until RSTB pin goes to high, chip will be started to initial, and playback “beep” tone to indicate enter idle mode.

User can get less current consumption by control RSTB pin specially in some application which concern standby current.

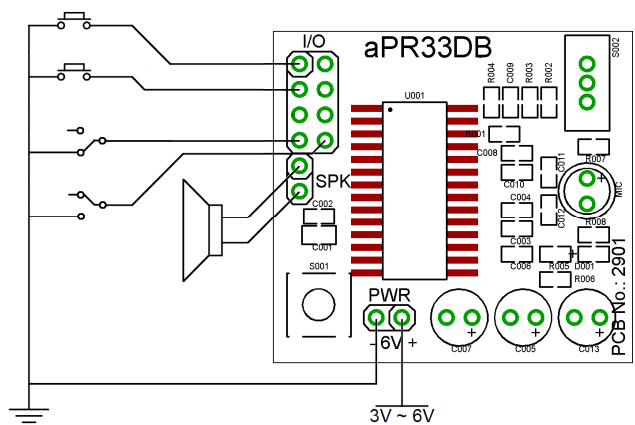


■ **EXAMPLE**

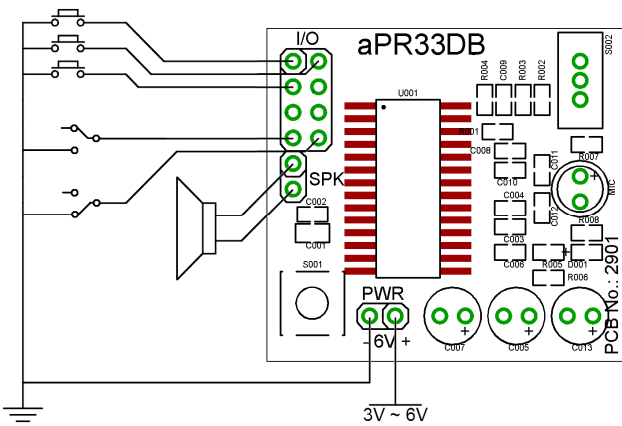
The aPR33DB is one of the simplest solutions for achieve tape mode demo. The circuit board already includes the peripheral circuit which containing microphone. Developers only need to notice how to connect with their development environment. It can effectively decrease the time of circuit connecting & any possible mistakes. Below figure shows how to connect aPR33DB with external key in tape mode:



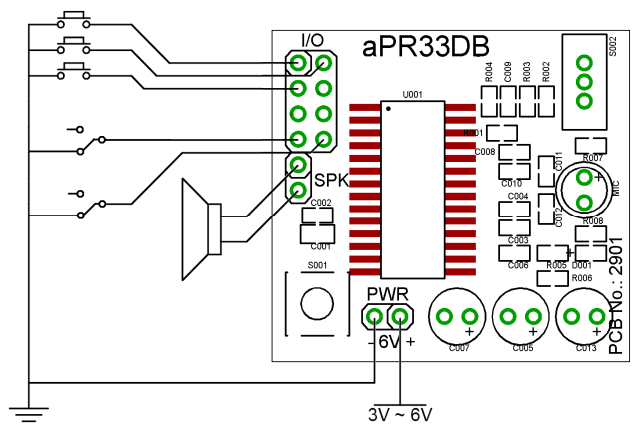
⊙ Auto Rewind option & Beep is ON.



⊙ Auto Rewind option & Beep is OFF.



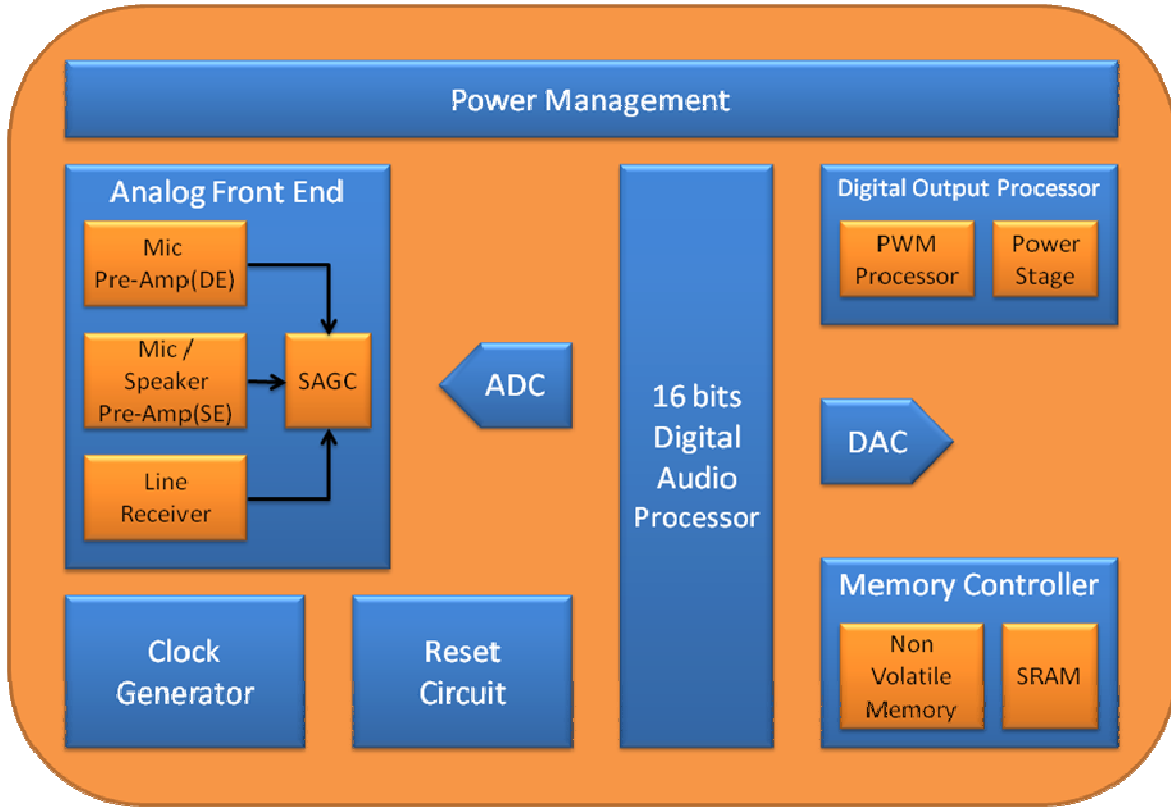
⊙ Non-Auto Rewind option & Beep is ON.



⊙ Non-Auto Rewind option & Beep is OFF.

■ **BLOCK DIAGRAM**

Figure 1. Block Diagram



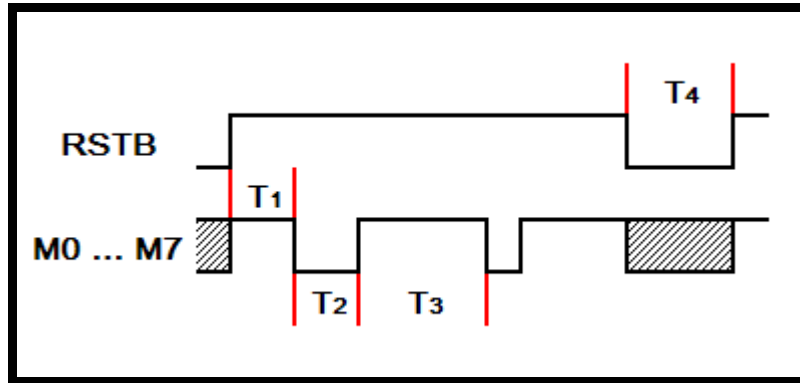
■ **ABSOLUTE MAXIMUM RATINGS**

Symbol	Rating	Unit
VDD – VSS	-0.3 ~ +10.0	V
V <sub>IN</sub>	VSS-0.3 < V <sub>IN</sub> < VDD+0.3	V
V <sub>OUT</sub>	VSS < V <sub>OUT</sub> < VDD	V
T(Operating)	-40 ~ +85	°C
T(Junction)	-40 ~ +125	°C
T(Storage)	-40 ~ +125	°C

## ■ DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	3.0		6.5	V	
IsB	Standby Current			1	μA	
IPDN	Power-Down Current		15	20	μA	
IOP(IDLE)	Operating Current (Idle)		20		mA	VDD = 5V
IOP(REC)	Operating Current (Record)		35		mA	VDD = 5V
IOP(PLAY)	Operating Current (Playback)		25		mA	VDD = 5V
VIH	"H" Input Voltage	2.5			V	
VIL	"L" Input Voltage			0.6	V	
IVOUT	VOUT Current		185		mA	
IOH	O/P High Current		8		mA	VDD = 5V / VOH=4.5V
IOL	O/P Low Current		14		mA	VDD = 5V / VOH=0.5V
RNPIO	Input pin pull-down resistance		300		KΩ	External floating or drive low.
			1		MΩ	External drive high.
RUPIO	Input pin pull-up resistance		4.7		KΩ	
△Fs/Fs	Frequency stability			5	%	VDD = 5V ± 1.0V
△Fc/Fc	Chip to chip Frequency Variation			5	%	Also apply to lot to lot variation.

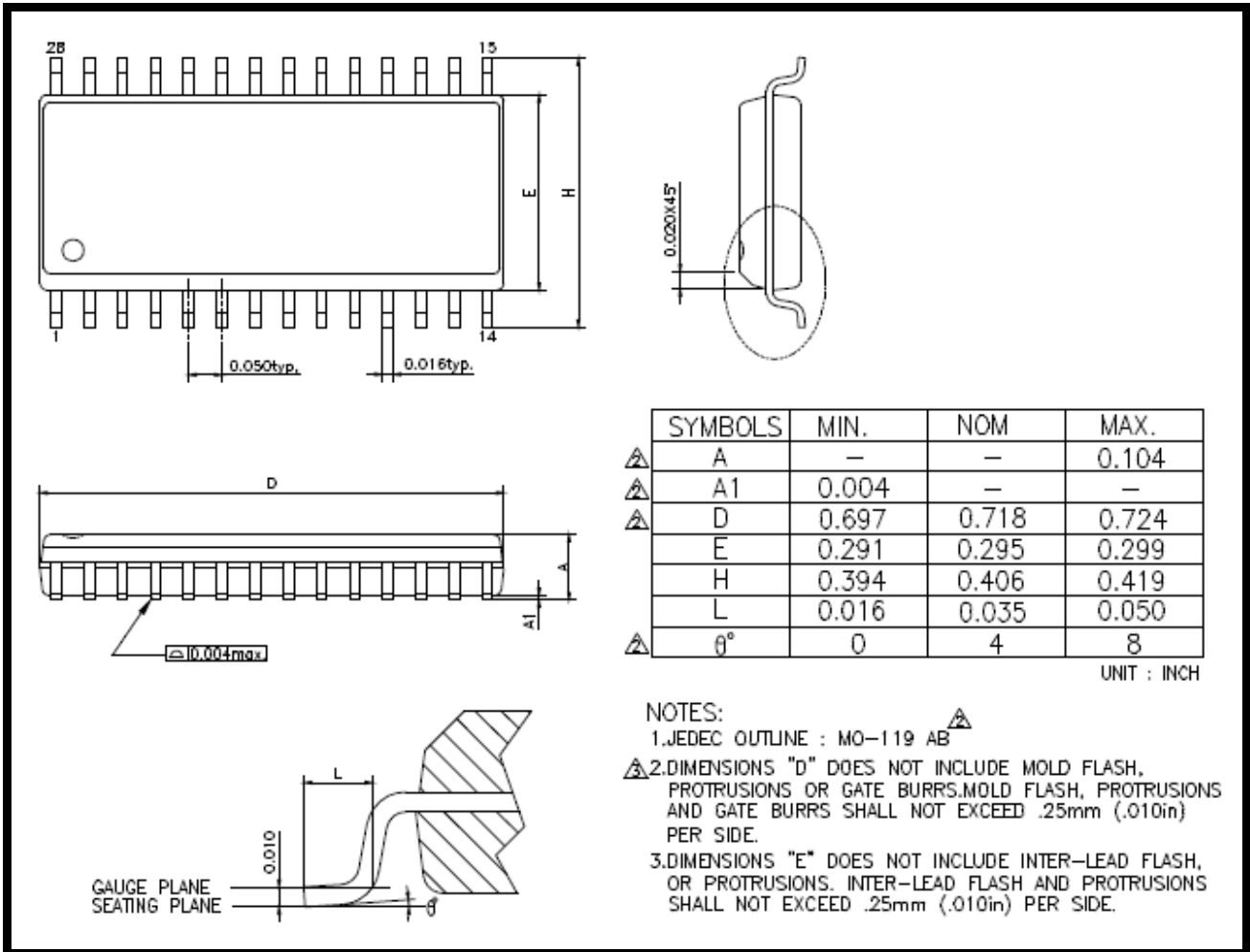
■ AC CHARACTERISTICS



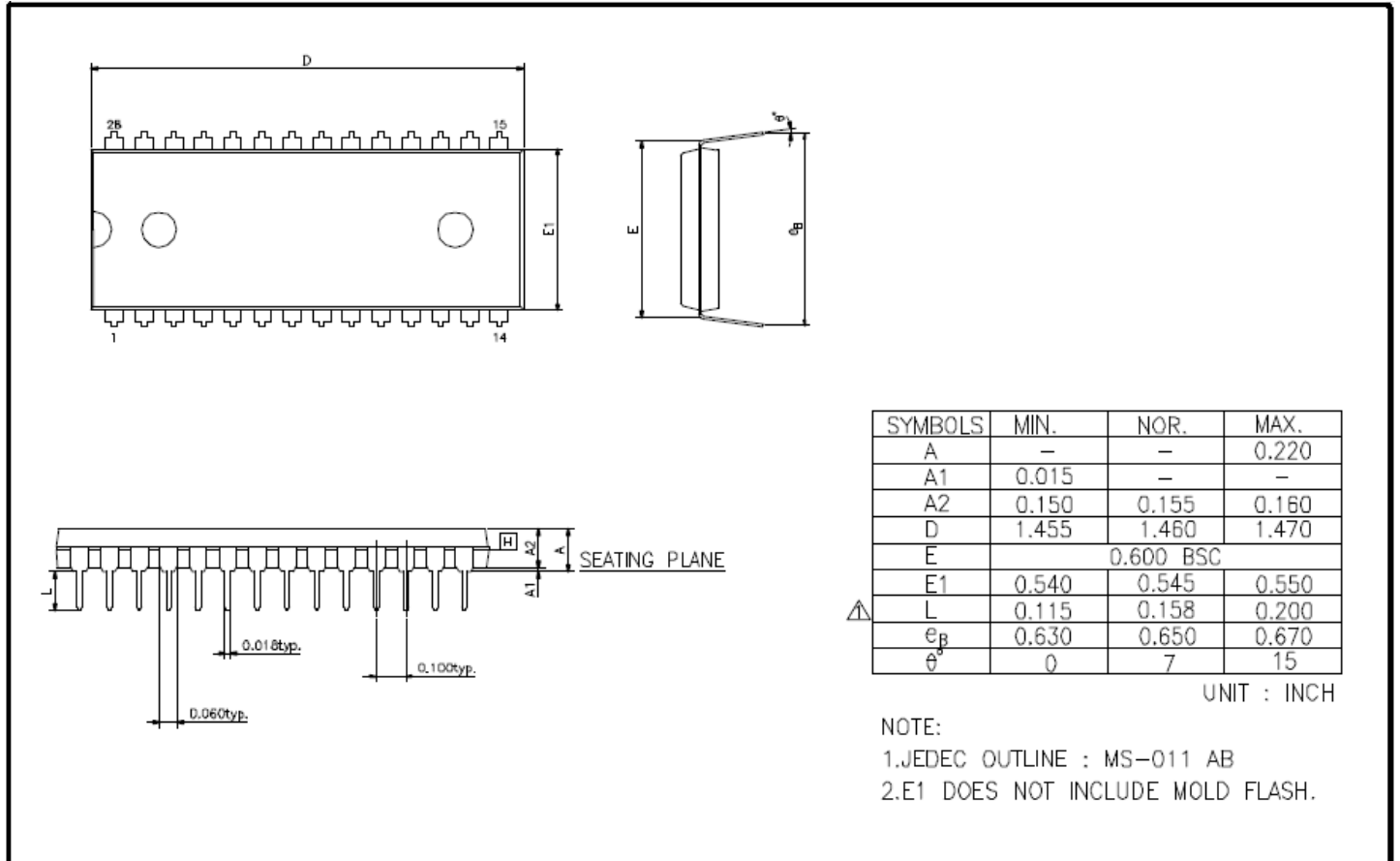
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	/CS Setup Time	100	--	--	mS	VDD=5.0V
T2	Trigger Setup Time	16	--	--	mS	VDD=5.0V
T3	Trigger Hold Time	16	--	--	mS	VDD=5.0V
T4	/CS Hold Time	100	--	--	uS	VDD=5.0V



■ **PACKAGE INFORMATION**  
**28Pin 300mil SOP Package**



**28Pin 600mil DIP Package**



■ **HISTORY**

**Ver. E**

Delete aPR33A1 data.

---

**Ver. D**

Modify Page. 11 -12 line in circuit

---

**Ver. C**

Modify PAGE. 7 - 10 “connect” → add

---

**Ver. B (2013/06/07)**

Add DIP Package and outline

Delete data of aPR33A2

---

**Ver. A (2013/03/29)**

- Original version data sheet for aPR33Ax -C3.1.