

Features

- Low power consumption
- Built-in hysteresis characteristic
- Low temperature coefficient
- TO-92 & SOT-89 package
- Built-in high-stability reference source

Applications

- Battery checkers
- Microcomputer reset
- Level selectors
- Battery memory backup
- Power failure detectors
- Non-volatile RAM signal storage protectors

General Description

The HT70XX series is a set of three-terminal low power voltage detectors implemented in CMOS technology. Each voltage detector in the series detects a particular fixed voltage ranging from 2.2V to 7V. The voltage detectors consist of a high-precision and low power consumption standard voltage source, a comparator, hysteresis circuit, and an output driver. CMOS technology ensures low power consumption.

Although designed primarily as fixed voltage detectors, these devices can be used with external components to detect user specified threshold voltages (NMOS open drain type only).

Selection Table

Part No.	Detectable Voltage	Hysteresis Width	Tolerance
HT7022A	2.2V	0.11V	±5%
HT7024A	2.4V	0.12V	±5%
HT7027A	2.7V	0.135V	±5%
HT7033A	3.3V	0.165V	±5%
HT7039A	3.9V	0.195V	±5%
HT7044A	4.4V	0.22V	±5%
HT7050A	5.0V	0.25V	±5%
HT7070A	7.0V	0.35V	±5%

Note: The output type selection codes are:

NMOS open drain normal open, active low

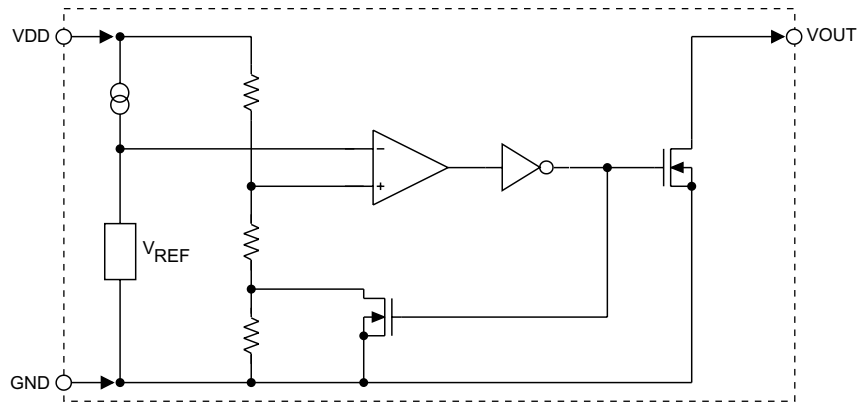
For example: The HT7070A is a 7.0V, NMOS open drain active low output

Output type selection table

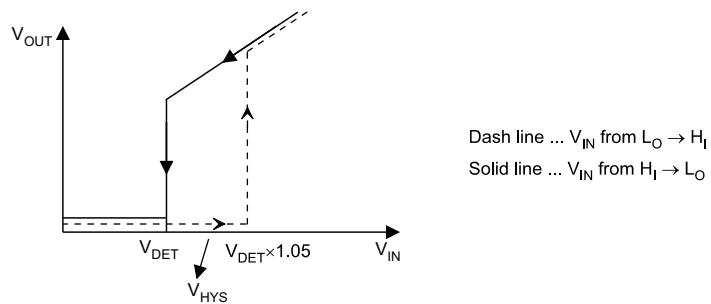
Type	V _{DD}		V _{DD} > V _{DET} (+)	V _{DD} ≤ V _{DET} (-)
	V _{OUT}			
A			Hi-Z	VSS

Block Diagram

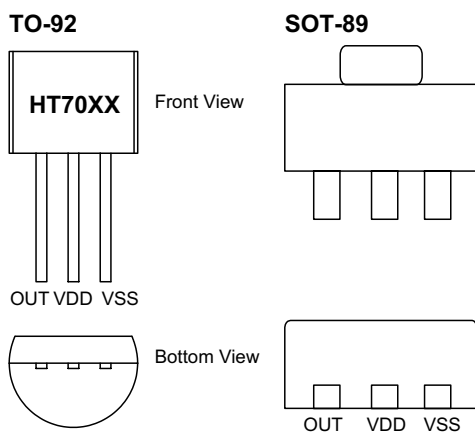
N channel open drain output (normal open; active low)

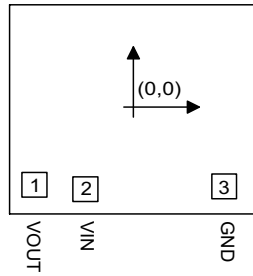


A type



Pin Assignment



Pad Assignment
HT70XX (except HT7022A)

 Chip size: $1317 \times 1158 \text{ (}\mu\text{m)}^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates
HT70XX (except HT7022A)

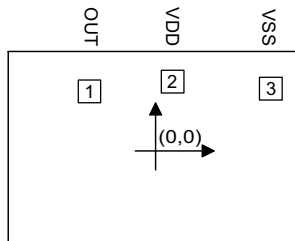
 Unit: μm

Pad No.	X	Y
1	-483.30	-379.50
2	-234.60	-399.50
3	443.90	-386.00

HT7022A only

 Unit: μm

Pad No.	X	Y
1	-434.34	394.97
2	120.65	461.01
3	774.70	412.75

HT7022A only

 Chip size: $2032 \times 1321 \text{ (}\mu\text{m)}^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Absolute Maximum Ratings

Supply Voltage, except HT7022A.....	$V_{SS}-0.3\text{V}$ to $V_{SS}+26\text{V}$
Supply Voltage, HT7022A only.....	-0.3V to 13V
Output Voltage.....	$V_{SS}-0.3\text{V}$ to $V_{DD}+0.3\text{V}$
Storage Temperature.....	-50°C to 125°C
Operating Temperature.....	0°C to 70°C
Output Current.....	50mA
Power Consumption.....	200mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics
HT7022A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	2.09	2.2	2.31	V
	Lo→Hi Detectable Voltage	—	—	2.132	2.31	2.541	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	3.2V	No load	—	1.8	4	μA
V _{DD}	Operating Voltage	—	—	1.6	—	12	V
I _{OL}	Output Sink Current	2V	V _{OUT} =0.2V	0.5	1	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7024A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	2.28	2.4	2.52	V
	Lo→Hi Detectable Voltage	—	—	2.325	2.52	2.772	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	1.5	—	24	V
I _{OL}	Output Sink Current	2V	V _{OUT} =0.2V	0.5	1	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7027A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	2.565	2.7	2.835	V
	Lo→Hi Detectable Voltage	—	—	2.616	2.835	3.118	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	1.5	—	24	V
I _{OL}	Output Sink Current	2V	V _{OUT} =0.2V	0.5	1	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7033A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	3.135	3.3	3.465	V
	Lo→Hi Detectable Voltage	—	—	3.197	3.465	3.811	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	1.5	—	24	V
I _{OL}	Output Sink Current	2.5V	V _{OUT} =0.25V	1.2	2.5	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7039A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	3.705	3.9	4.095	V
	Lo→Hi Detectable Voltage	—	—	3.779	4.095	4.504	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	1.5	—	24	V
I _{OL}	Output Sink Current	2.5V	V _{OUT} =0.25V	1.2	2.5	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7044A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	4.18	4.4	4.62	V
	Lo→Hi Detectable Voltage	—	—	4.263	4.62	5.082	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	1.5	—	24	V
I _{OL}	Output Sink Current	3.6V	V _{OUT} =0.36V	3	6	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7050A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	4.75	5	5.25	V
	Lo→Hi Detectable Voltage	—	—	4.845	5.25	5.775	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	2.1	—	24	V
I _{OL}	Output Sink Current	3.6V	V _{OUT} =0.36V	3	6	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

HT7070A

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DET}	Hi→Lo Detectable Voltage	—	—	6.65	7	7.35	V
	Lo→Hi Detectable Voltage	—	—	6.783	7.35	8.085	V
V _{HYS}	Hysteresis Width	—	—	0.02 V _{DET}	0.05 V _{DET}	0.1 V _{DET}	V
I _{DD}	Operating Current	8V	No load	—	4	7	μA
V _{DD}	Operating Voltage	—	—	2.1	—	24	V
I _{OL}	Output Sink Current	5V	V _{OUT} =0.5V	5	10	—	mA
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	0°C<Ta<70°C	—	±0.9	—	mV/°C

Functional Description

The HT70XX series is a set of voltage detectors equipped with a high stability voltage reference which is connected to the negative input of a comparator—denoted as V_{REF} in the following figure for NMOS output voltage detector.

When the voltage drop to the positive input of the comparator (i.e, V_B) is higher than V_{REF}, V_{OUT} goes high, M1 turns off, and V_B is expressed as V_{BH}=V_{DD} × (R_B+R_C) / (R_A+R_B+R_C). If V_{DD} is decreased so that V_B falls to a value less than V_{REF}, the comparator output inverts from high to low, V_{OUT} goes low, V_C is high, M1 turns on, R_C is bypassed, and V_B becomes: V_{BL}=V_{DD}×R_B / (R_A+R_B), which is less than V_{BH}. By so doing, the comparator output will stay low to prevent the circuit from oscillating when V_B ≈ V_{REF}.

If V_{DD} falls below the minimum operating voltage, the output becomes undefined. When V_{DD} goes from low to V_{DD} × R_B / (R_A+R_B) > V_{REF}, the comparator output and V_{OUT} goes high.

The detectable voltage is defined as:

$$V_{DET} (-) = \frac{R_A + R_B + R_C}{R_B + R_C} \times V_{REF}$$

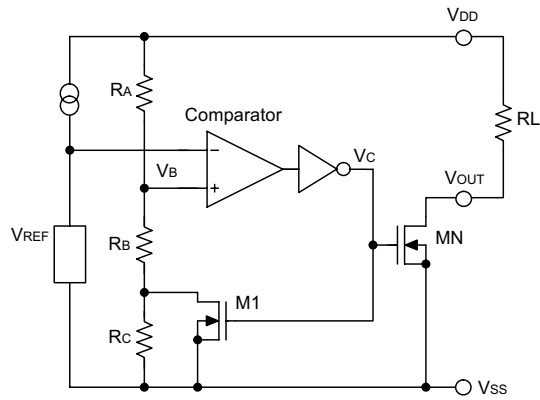
The release voltage is defined as:

$$V_{DET} (+) = \frac{R_A + R_B}{R_B} \times V_{REF}$$

The hysteresis width is:

$$V_{HYS} = V_{DET (+)} - V_{DET (-)}$$

The figure demonstrates the NMOS output type with positive output polarity (V_{OUT} is normally open, active low). The HT70XX series also supplies options for other output types with active high outputs. Application circuits shown are examples of positive output polarity (normally open, active low) unless otherwise specified.



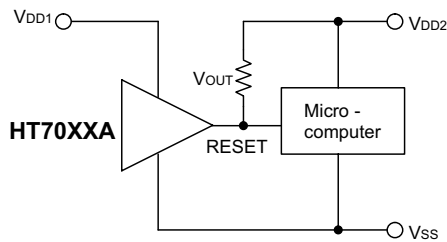
NMOS output voltage detector (HT70XXA)

Application Circuits

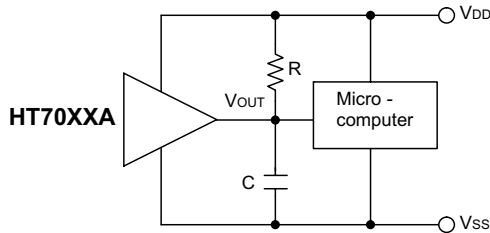
Microcomputer reset circuit

Normally a reset circuit is required to protect the micro-computer system from malfunctions due to power line interruptions. The following examples show how different output configurations perform a reset function in various systems.

- NMOS open drain output application for separate power supply

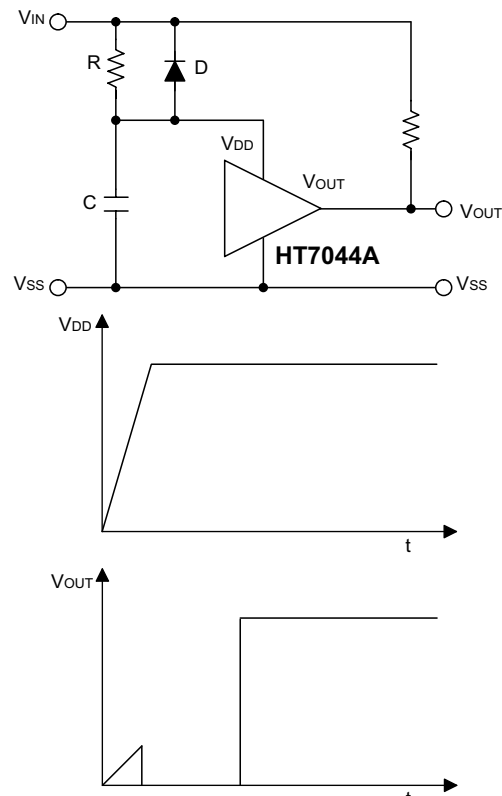


- NMOS open drain output application with R-C delay



Power-on reset circuit

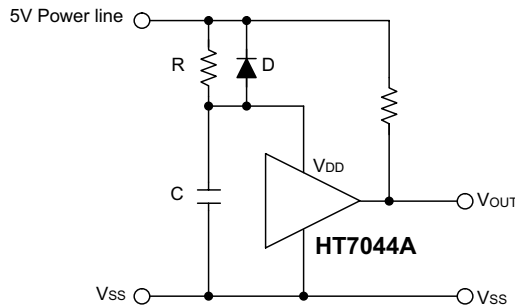
With several external components, the NMOS open drain type of the HT70XX series can be used to perform a power-on reset function as shown:



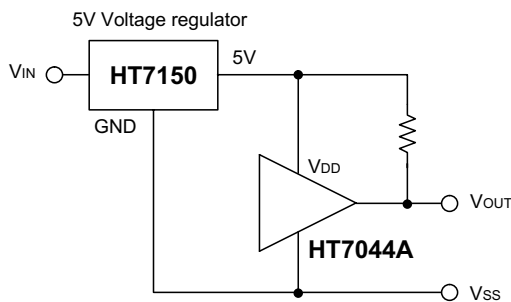
5V power line monitoring circuit

Generally, a minimum operating voltage of 4.5V is guaranteed in a 5V power line system. The HT7044A is recommended for use as 5V power line monitoring circuit.

- 5V power line monitor with power-on reset



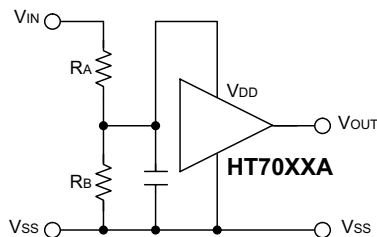
- with 5V voltage regulator



Change of detectable voltage

If the required voltage is not found in the standard product selection table, it is possible to change it by using external resistance dividers or diodes.

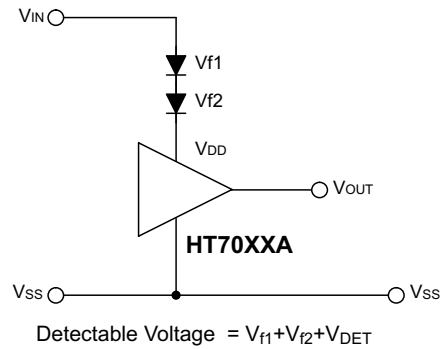
- Varying the detectable voltage with a resistance divider



$$\text{Detectable voltage} = \frac{R_A + R_B}{R_B} \times V_{DET}$$

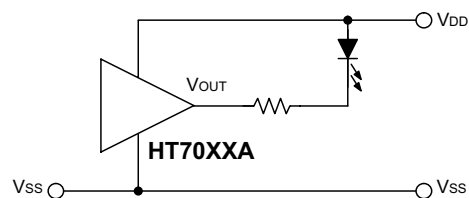
$$\text{Hysteresis width} = \frac{R_A + R_B}{R_B} \times V_{HYS}$$

- Varying the detectable voltage with a diode



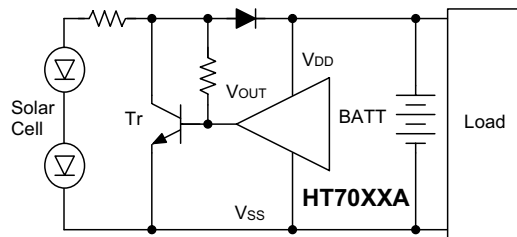
Malfunction analysis

The following circuit demonstrates the way a circuit analyzes malfunctions by monitoring the variation or spike noise of power supply voltage.



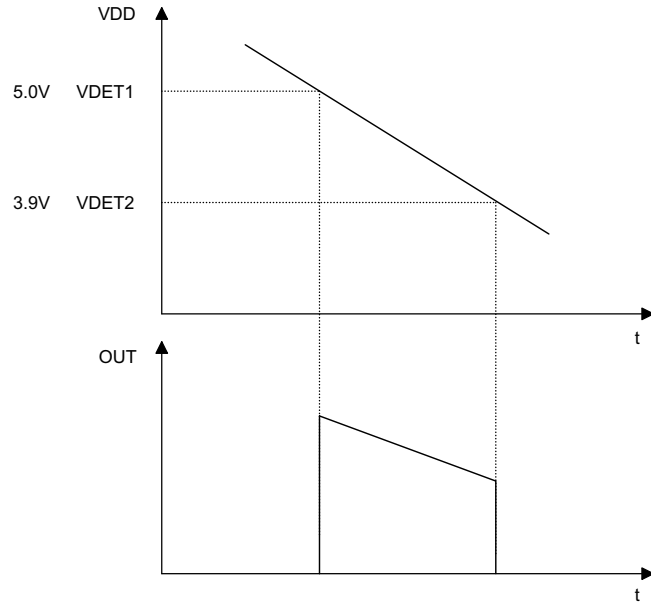
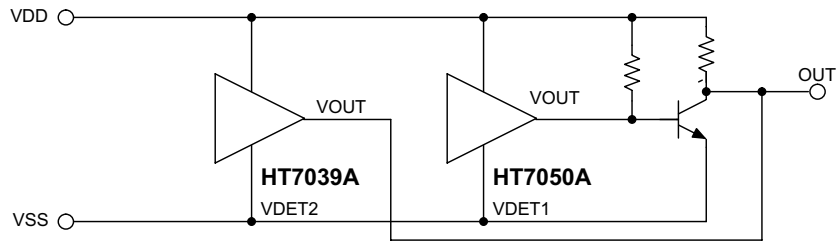
Charge monitoring circuit

The following circuit shows a charged monitor for protection against battery deterioration by overcharging. When the voltage of the battery is higher than the set detectable voltage, the transistor turns on to bypass the charge current, protecting the battery from overcharging.



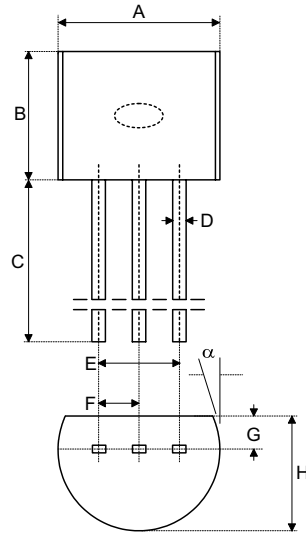
Level selector

The following diagram illustrates a logic level selector.



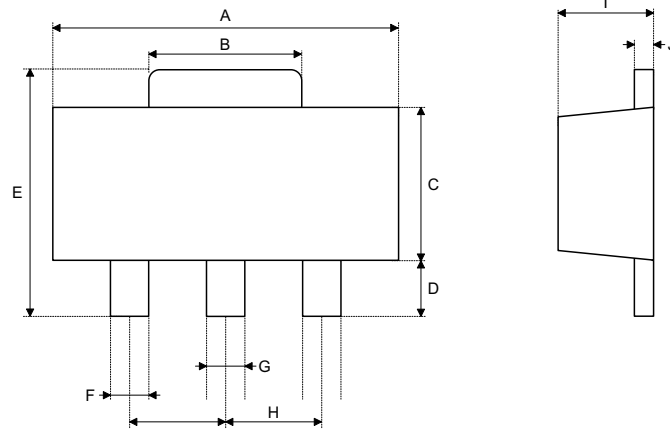
Package Information

3-pin TO-92 outline dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	170	—	200
B	170	—	200
C	500	—	—
D	11	—	20
E	90	—	110
F	45	—	55
G	45	—	65
H	130	—	160
I	8	—	18
α	4°	—	6°

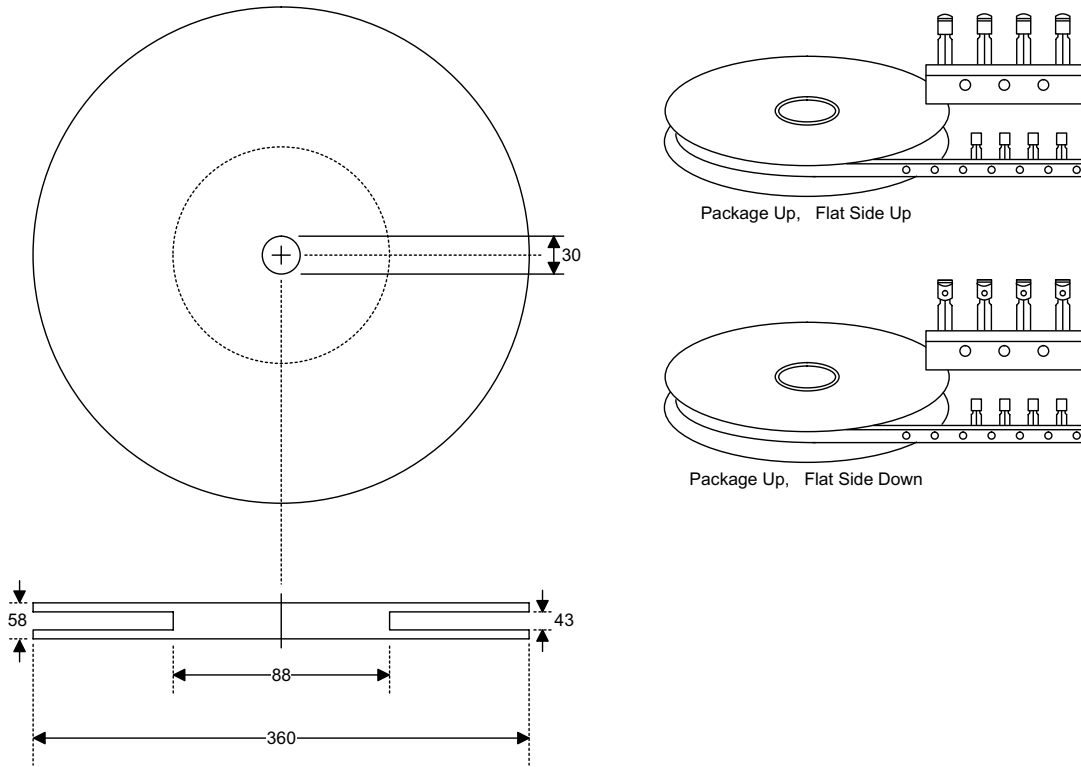
3-pin SOT-89 outline dimensions



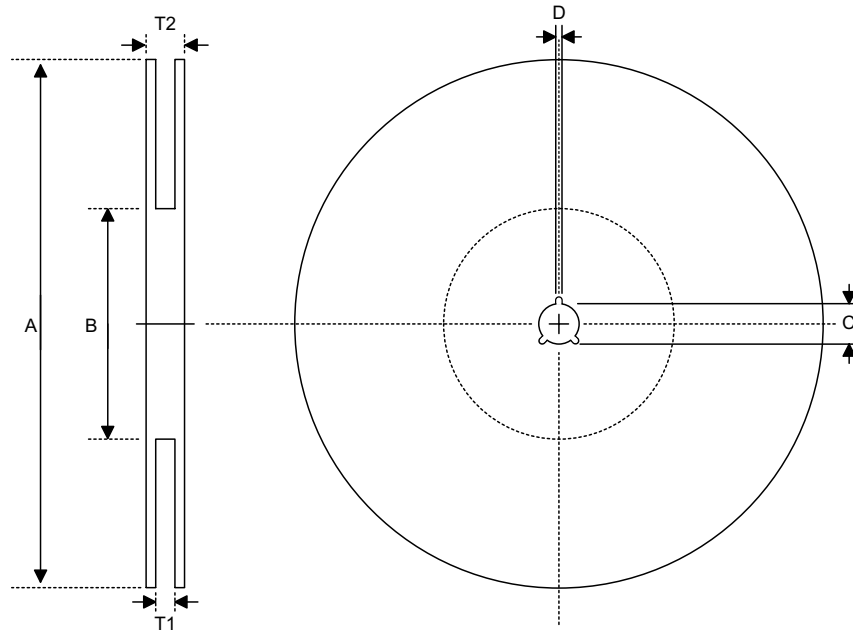
Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	173	—	181
B	64	—	72
C	90	—	102
D	35	—	47
E	155	—	167
F	14	—	19
G	17	—	22
H	—	59	—
I	55	—	63
J	14	—	17

Product Tape and Reel Specifications

TO-92 reel dimensions (Unit: mm)



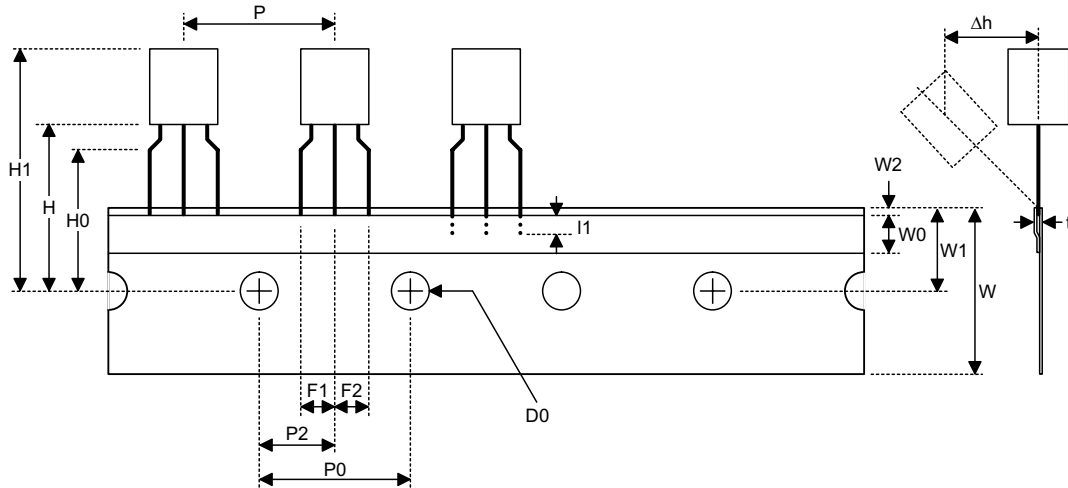
SOT-89 reel dimensions



SOT-89

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	180±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	12.75+0.15
D	Key Slit Width	1.9±0.15
T1	Space Between Flange	12.4+0.2
T2	Reel Thickness	17-0.4

TO-92 carrier tape dimensions



TO-92

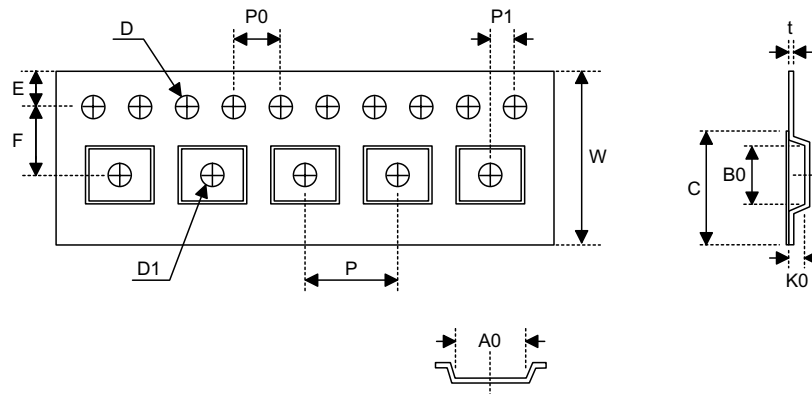
Symbol	Description	Dimensions in mm
l1	Taped Lead Length	(2.5)
P	Component Pitch	12.7±1.0
P ₀	Perforation Pitch	12.7±0.3
P ₂	Component to Perforation (Length Direction)	6.35±0.4
F ₁	Lead Spread	2.5+0.4 -0.1
F ₂	Lead Spread	2.5+0.4 -0.1
Δh	Component Alignment	0±0.1
W	Carrier Tape Width	18.0+1.0 -0.5
W ₀	Hold-down Tape Width	6.0±0.5
W ₁	Perforation Position	9.0±0.5
W ₂	Hold-down Tape Position	(0.5)
H ₀	Lead Clinch Height	16.0±0.5
H ₁	Component Height	Less than 24.7
D ₀	Perforation Diameter	4.0±0.2
t	Taped Lead Thickness	0.7±0.2
H	Component Base Height	19.0±0.5

Note: Thickness less than 0.38±0.05mm~0.5mm

P₀ Accumulated pitch tolerance: ±1mm/20pitches.

() Bracketed figures are for consultation only

SOT-89 carrier tape dimensions



SOT-89

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.05
D	Perforation Diameter	1.5+0.1
D1	Cavity Hole Diameter	1.5+0.1
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.10
A0	Cavity Length	4.8±0.1
B0	Cavity Width	4.5±0.1
K0	Cavity Depth	1.8±0.1
t	Carrier Tape Thickness	0.30±0.013
C	Cover Tape Width	9.3

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