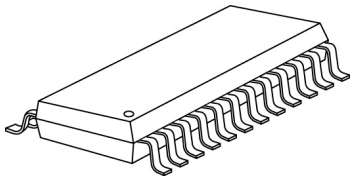
16-Channel PWM-Embedded LED Driver

Features

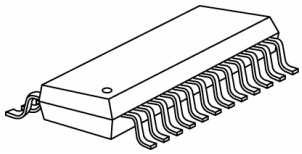
- Backward compatible with MBI5026 in package
- 16 constant-current output channels
- 12-bit color depth PWM control
- Scrambled-PWM technology to improve refresh rate
- Open/Short-Circuit Detection to detect individual LED errors
- 8-bit programmable output current gain
- Constant output current range:
  5 ~ 60mA at 3.3V supply voltage
  5 ~ 80mA at 5.0V supply voltage
- Output current accuracy:
  between channels: <±1.5% (typ.), and
  between ICs: <±3.0% (typ.)
- Staggered output delay
- Maximum data clock frequency: 25MHz
- Schmitt trigger input
- 3.0V-5.5V supply voltage

Small Outline Package



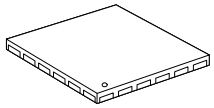
GF: SOP24-300-1.00

Thin Shrink SOP



GTS: TSSOP24-173-0.65

Quad Flat No-Lead



GFN: QFN24-4*4-0.5

Product Description

MBI5031 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with 12-bit color depth. MBI5031 features a 16-bit shift register which converts serial input data into each 12-bit pixel gray scale of output port. At MBI5031 output port, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of Vf variations. The output current can be preset through an external resistor. Moreover, the preset current of MBI5031 can be further programmed to 256 gain steps for LED global brightness adjustment.

With Scrambled-PWM (S-PWM™) technology, MBI5031 enhances Pulse Width Modulation by scrambling the “on” time into several “on” periods. The enhancement equivalently increases the visual refresh rate. When building a 12-bit color depth video, S-PWM™ reduces the flickers and improves the fidelity. MBI5031 offloads the signal timing generation of the host controller which just needs to feed data into drivers. MBI5031 drives the corresponding LEDs to the brightness specified by image data. With MBI5031, all output channels can be built with 12-bit color depth (4,096 gray scales).

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Block Diagram

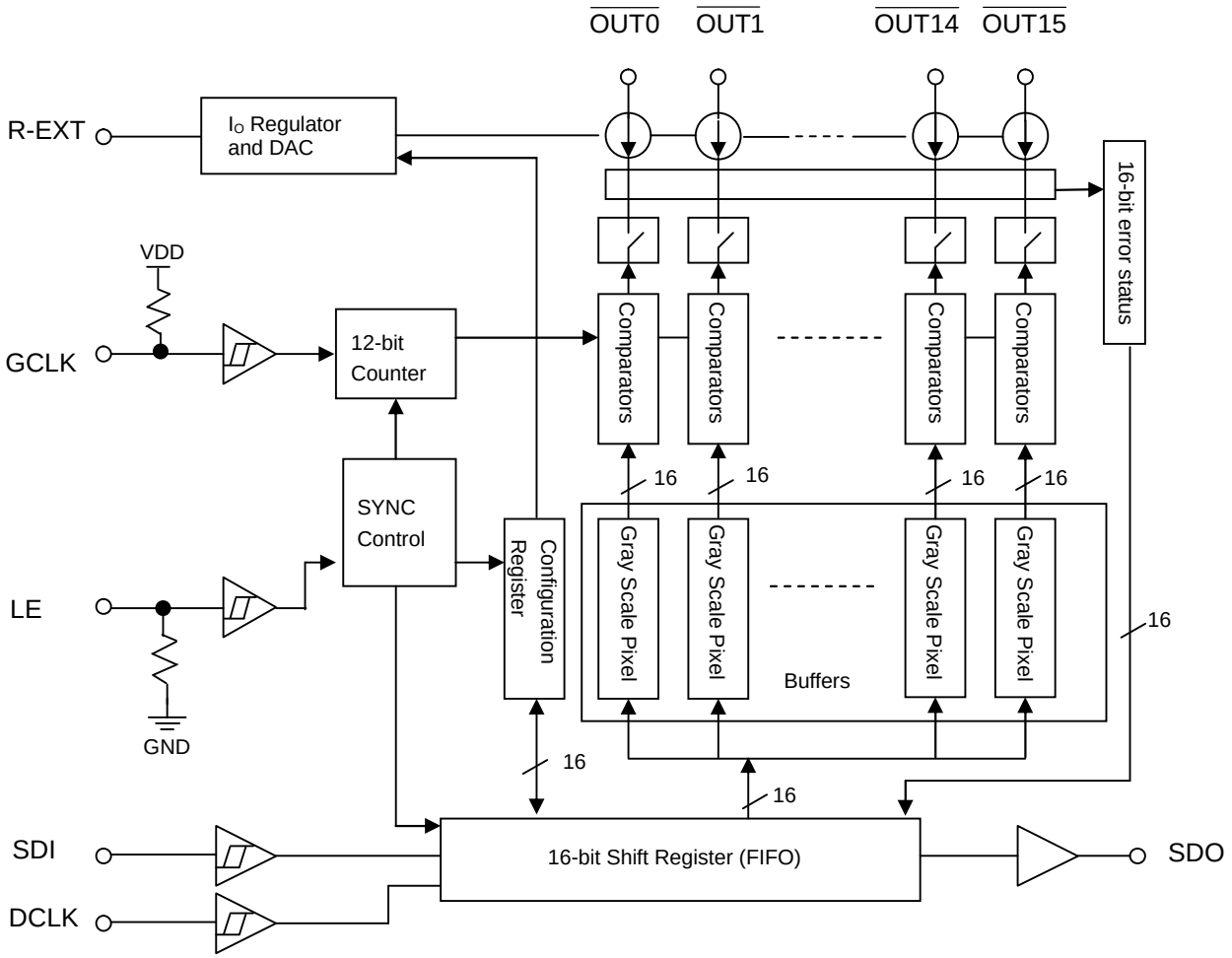
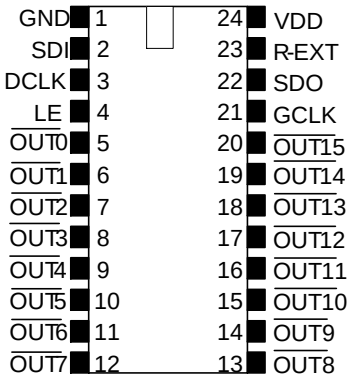
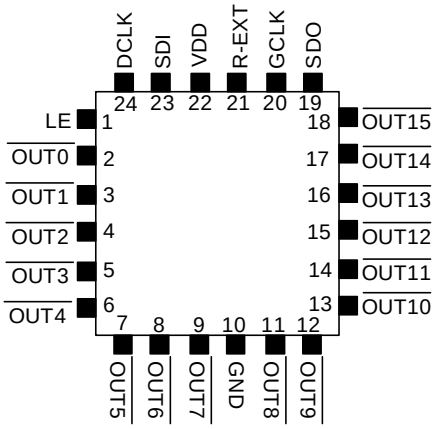


Figure 1

Pin Configuration



MBI5031GF/GTS



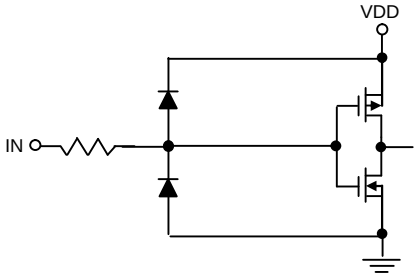
MBI5031GFN

Terminal Description

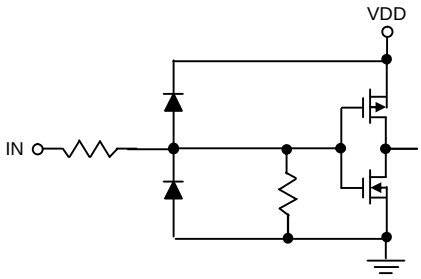
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock comparing with input data.
SDO	Serial-data output to the receiver-end SDI of next driver IC
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

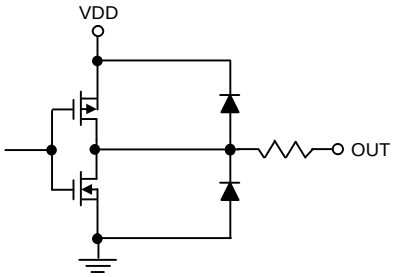
GCLK, DCLK, SDI terminal



LE terminal



SDO terminal



Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	7	V
Input Pin Voltage (SDI)		V_{IN}	-0.4~V_{DD}+0.4	V
Output Current		I_{OUT}	+80	mA
Sustaining Voltage at OUT Port		V_{DS}	17	V
Data Clock Frequency*		F_{DCLK}	+25	MHz
Gray Scale Clock Frequency		F_{GCLK}	+25	MHz
GND Terminal Current		I_{GND}	+1280	mA
Power Dissipation (On PCB, Ta=25°C)	GF Type	P_D	2.39	W
	GTS Type		3.87	
	GFN Type		3.49	
Thermal Resistance (On PCB, Ta=25°C)	GF Type	$R_{th(j-a)}$	52.37	°C/W
	GTS Type		32.34	
	GFN Type		35.85	
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C

***** Supply Voltage is 5V.

Electrical Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		5	-	80	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=10.8mA V_{DS}=1.0V	R_{ext}=910Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=10.8mA V_{DS}=1.0V	R_{ext}= 910Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=460Ω@21mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1.0	±5.0	% / V
LED Error Detection Threshold		$V_{DS,TH}$	-		-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.3	4.3	mA
		I_{DD}(off) 2	R_{ext}=910Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.0	9.0	
		I_{DD}(off) 3	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	6.6	9.6	
	"On"	I_{DD}(on) 1	R_{ext}=910Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.2	10.2	
		I_{DD}(on) 2	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.3	12.3	

Electrical Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		5	-	60	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3*V_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		2.9	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=10.5mA V_{DS}=1.0V	R_{ext}=910Ω	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=10.8mA V_{DS}=1.0V	R_{ext}=910Ω	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=460Ω@21mA		-	±0.1	±0.5	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±5.0	% / V
LED Error Detection Threshold		$V_{DS,TH}$	-		-	0.15	0.20	V
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	2.0	4.0	mA
		I_{DD}(off) 2	R_{ext}=910Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.0	7.0	
		I_{DD}(off) 3	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off		-	4.8	7.8	
	"On"	I_{DD}(on) 1	R_{ext}=910Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	7.2	10.2	
		I_{DD}(on) 2	R_{ext}=460Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$ =On		-	9.3	12.3	

Test Circuit for Electrical Characteristics

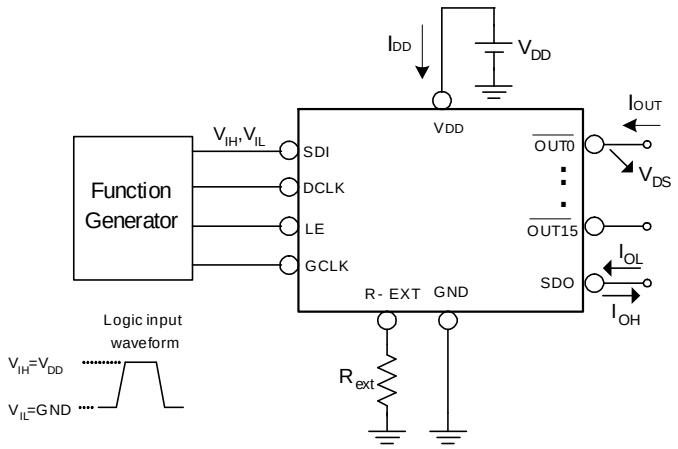


Figure 2

Switching Characteristics (V_{DD}=5.0V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=460Ω V_{LED}=4.5V R_L=152Ω C_L=10pF C_1=100nF C_2=10μF	1	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK - SDO	t_{PD0}		-	30	40	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	100	-	ns
	LE – SDO**	t_{PD2}**		-	30	40	ns
Stagger Delay Time	$\overline{OUT4n+1}$*	t_{DL1}		-	40	-	ns
	$\overline{OUT4n+2}$*	t_{DL2}		-	80	-	ns
	$\overline{OUT4n+3}$*	t_{DL3}		-	120	-	ns
Pulse Width	LE	$t_{W(L)}$		5	-	-	ns
	DCLK	$t_{W(DCLK)}$		20	-	-	ns
	GCLK	$t_{W(GCLK)}$		20	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	90	-	ns
Output Fall Time of Output Ports		t_{OF}		-	70	-	ns
Error Detection Minimum Duration		t_{EDD}***		-	1	-	μs

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 6.

Switching Characteristics (V_{DD}=3.3V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=460Ω V_{LED}=4.5V R_L=152Ω C_L=10pF C_1=100nF C_2=10μF	1	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		1	-	-	ns
	LE ↓ – DCLK ↑	t_{SU2}		5	-	-	ns
Hold Time	DCLK ↑ - SDI	t_{H0}		3	-	-	ns
	DCLK ↑ - LE ↓	t_{H1}		7	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	45	50	ns
	GCLK – $\overline{OUT4n}$ *	t_{PD1}		-	120	-	ns
	LE – SDO	t_{PD2}**		-	45	50	ns
Stagger Delay Time	$\overline{OUT4n+1}$*	t_{DL1}		-	40	-	ns
	$\overline{OUT4n+2}$*	t_{DL2}		-	80	-	ns
	$\overline{OUT4n+3}$*	t_{DL3}		-	120	-	ns
Pulse Width	LE	$t_{W(L)}$		5	-	-	ns
	DCLK	$t_{W(DCLK)}$		25	-	-	ns
	GCLK	$t_{W(GCLK)}$		20	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	90	-	ns
Output Fall Time of Output Ports		t_{OF}		-	70	-	ns
Error Detection Minimum Duration		t_{EDD}***		-	1	-	μs

* Refer to the Timing Waveform, where n=0, 1, 2, 3.

**In timing of “Read Configuration” and “Read Error Status Code”, the next DCLK rising edge should be t_{PD2} after the falling edge of LE.

***Refer to Figure 6.

Test Circuit for Switching Characteristics

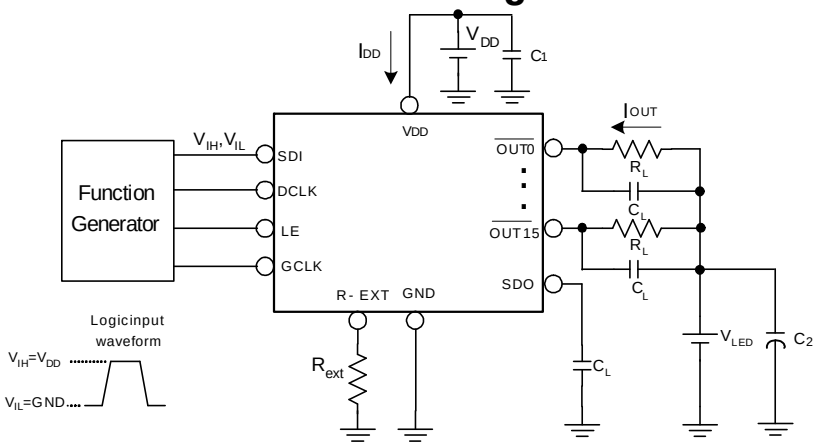
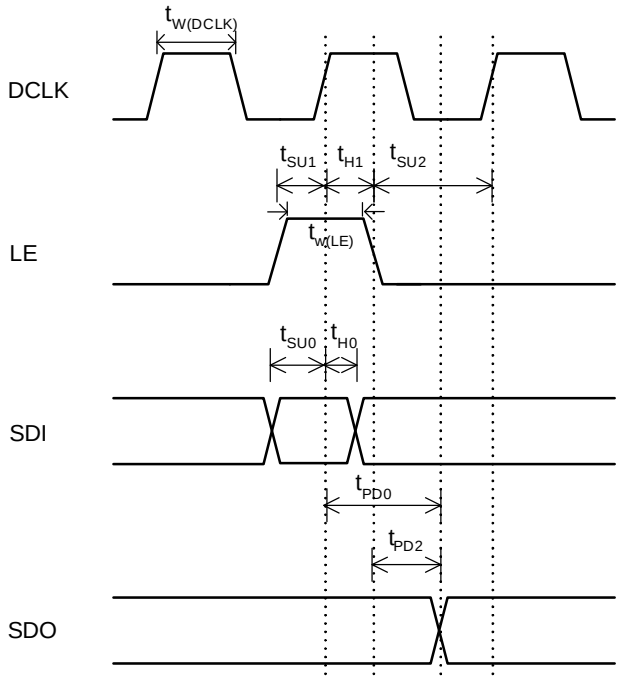


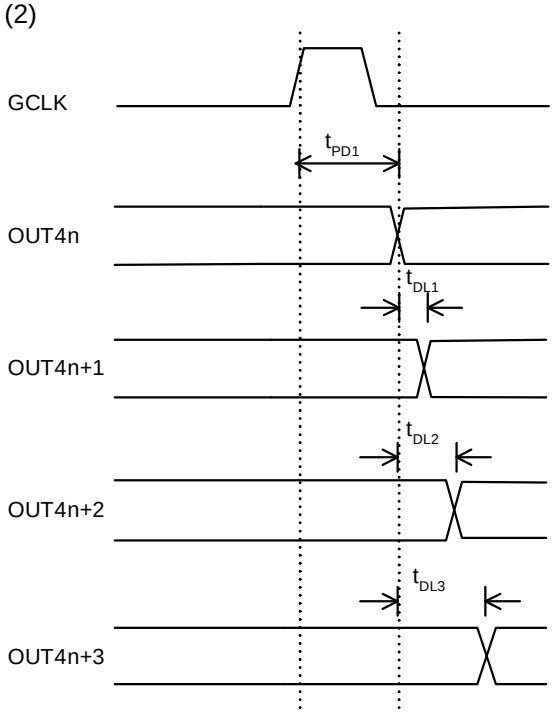
Figure 3

Timing Waveform

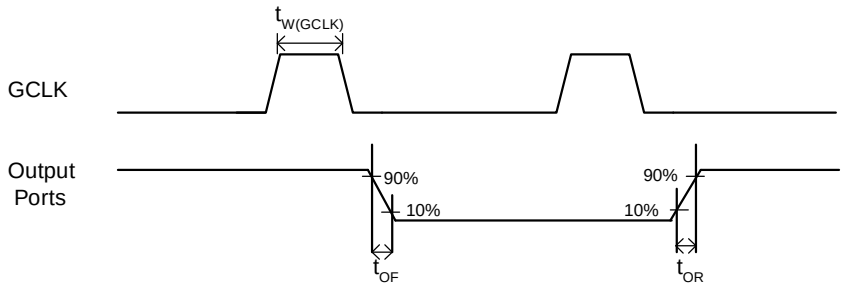
(1)



(2)



(3)

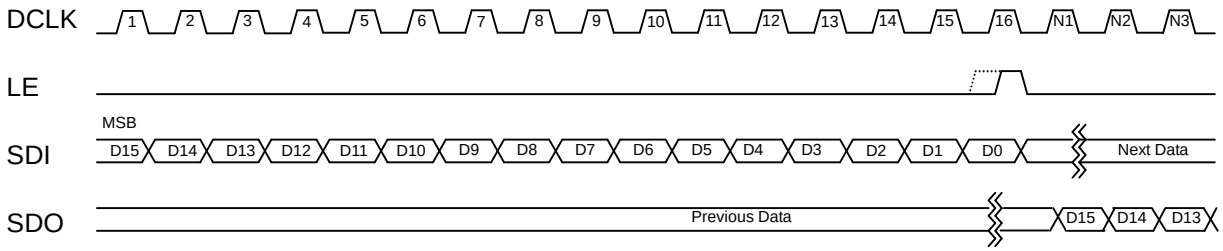


Principle of Operation

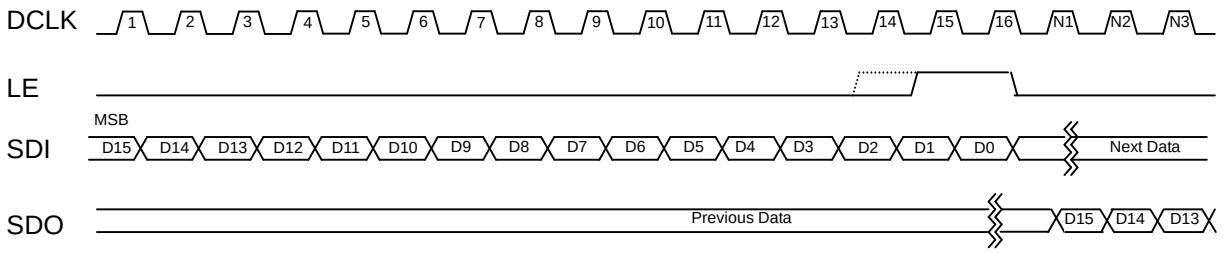
Control Command

	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**The Action after a Falling Edge of LE**
Data Latch	High	0 or 1	Serial data are transferred to the buffers
Global Latch	High	2 or 3	Buffer data are transferred to the comparators
Read Configuration	High	4 or 5	Move out “configuration register” to the shift registers
Enable “Error detection”	High	6 or 7	Detect the status of each output’s LED
Read “Error status code”	High	8 or 9	Move out “error status code” of 16 outputs to the shift registers
Write Configuration	High	10 or 11	Serial data are transferred to the “configuration register”

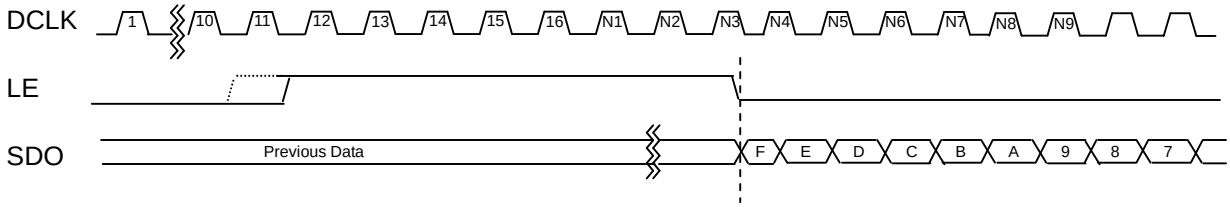
Data Latch



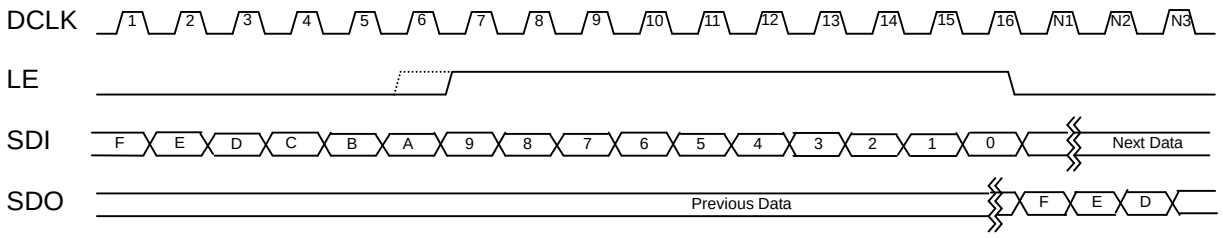
Global Latch



Read Configuration



Write Configuration



Setting Gray Scales of Pixels

MBI5031 implements the gray level of each output port using the S-PWM™ control algorithm. With the 16-bit data, all output channels can be built with 4,096 gray scales. The 16-bit input shift register latches 15 times of the gray scale data into each data buffer with a "data latch" command sequentially. With a "global latch" command for the 16th gray scale data, the 256-bit data buffers will be clocked in with the MSB first, loading the data from port 15 to port 0.

Full Timing for Data Loading

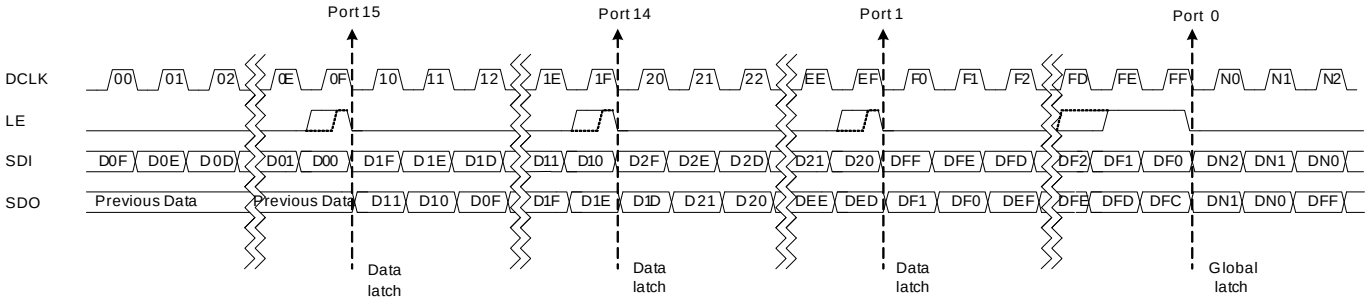


Figure 4

Open-Circuit Detection Principle

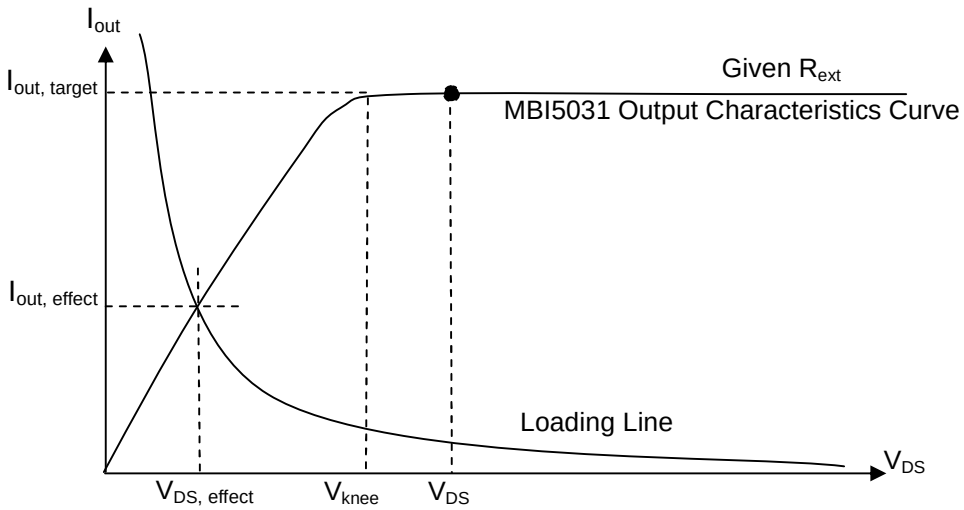


Figure 5

The principle of MBI5031 LED Open-Circuit Detection is based on the fact that the LED loading status is judged by comparing the effective current value ($I_{out,\ effect}$) of each output port with the target current ($I_{out,\ target}$) set by R_{ext}. As shown in the above figure, the knee voltage (V_{knee}) is the one between triode region and saturation region. The cross point between the loading line and MBI5031 output characteristics curve is the effective output point ($V_{DS,\ effect}$, $I_{out,\ effect}$).Thus, after the command of "enabling error detection", the output ports of MBI5031 will be turned on for a while. It is required to obtain the stable error status result for 1μ second. Then, the error status saved in the built-in register would be shifted out through SDO pin bit by bit by sending the command of "Read Error Status Code". Thus, to detect the status of LED correctly, the output ports of MBI5031 must be turned on. The relationship between the Error Status code and the effective output point is shown below:

State of Output Port	Condition of Effective Output Point	Detected Open-Circuit Error Status Code	Meaning
Off	$I_{out,\ effect} = 0$	"0"	-
On	$I_{out,\ effect} \leqq I_{out,\ target}$ and $V_{out,\ effect} < V_{DS,\ TH}$	"1"	Open Circuit
	$I_{out,\ effect} = I_{out,\ target}$ and $V_{out,\ effect} \geqq V_{DS,\ TH}$	"0"	Normal

Short-Circuit Detection Principle

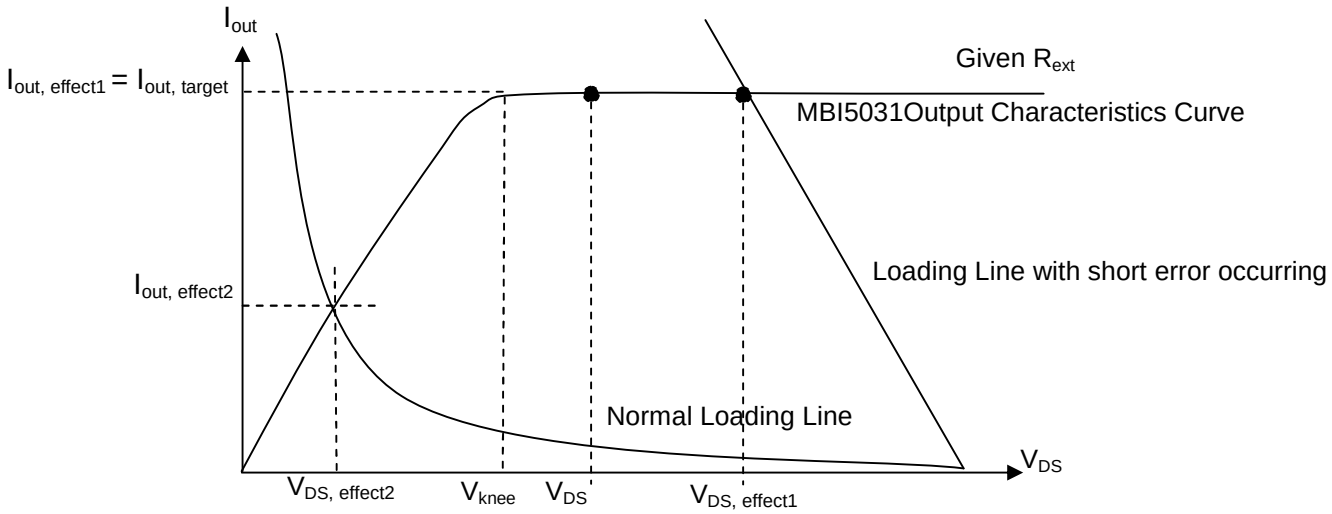
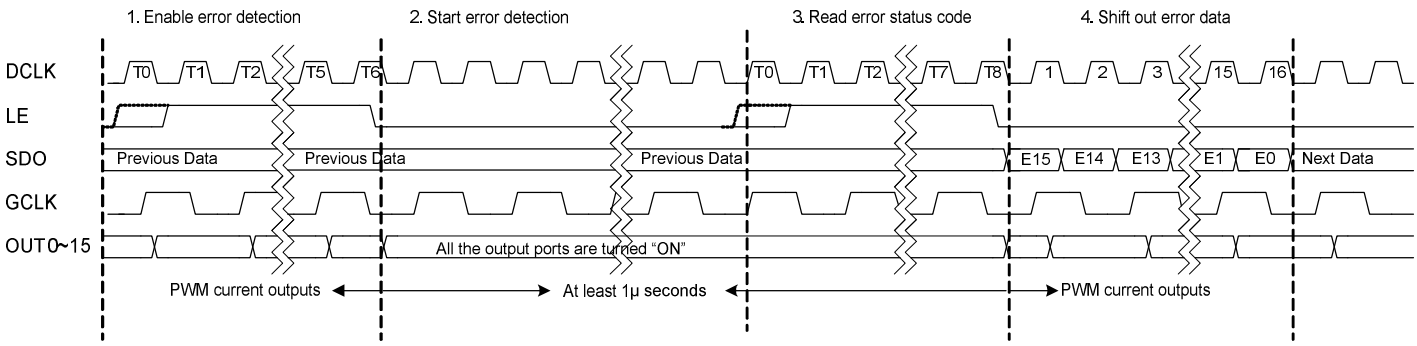


Figure 6

When LED is damaged, a short-circuit error may occur. To effectively detect the short-circuit error, LEDs need insufficiently biasing. The principle of MBI5031 LED Short Circuit Detection is based on the fact that the LED loading status is judged by comparing the effective current value($I_{out, effect}$) of each output port with the target current($I_{out, target}$) set by R_{ext}. When LED is short and the LED forward voltage drops at the output point, $V_{DS,effect}$ will be larger than $V_{DS,TH}$; therefore, the detected short-circuit error status code will be “0”. When normal LED is insufficiently biased, its effective output point would be located at the ramp area of MBI5031 Output Characteristics Curve, compared with LED with a short error falling within the flat zone. The relationship between the Error Status code and the effective output point is shown below:

State of Output Port	Condition of Effective Output Point	Detected Short-Circuit Error Status Code	Meaning
OFF	$I_{out, effect} = 0$	“0”	-
ON	$I_{out, effect} \leqq I_{out, target}$ and $V_{DS, effect} < V_{DS, TH}$	“1”	Normal
	$I_{out, effect} = I_{out, target}$ and $V_{DS, effect} \geqq V_{DS, TH}$	“0”	Short Circuit



Note :
t_{EDD} = 1μs is required to obtain the stable error status result.

Figure 7

Definition of Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g.. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
X	0	1	11		1	8'b10101011								0	0

Bit	Attribute	Definition	Value	Function
F	Read	X	X	Reserved bit
E	Read	Thermal error flag	0 (Default)	Safe (OK)
			1	Over temperature (>150°C typ.)
D	Read	X	1	Reserved bit
C	Read/Write	PWM counting mode selection	00	64 times of MSB* 6-bit PWM counting plus once of LSB* 6-bit PWM counting
			01	16 times of MSB 6-bit PWM counting by 1/4 GCLK plus once of LSB 6-bit PWM counting
B			10	4 times of MSB 6-bit PWM counting by 1/16 GCLK plus once of LSB 6-bit PWM counting
			11 (Default)	12-bit PWM counting
A	Read/Write	PWM data synchronization mode	0	Auto-synchronization
			1 (Default)	Manual synchronization
9~2	Read/Write	Current gain adjustment	00000000 ~ 11111111	8'b10101011 (Default)
1	Read/Write	Thermal protection	0 (Default)	Disable
			1	Enable** , 25% of setting output current if T_{TF} > 150°C
0	Read/Write	Time-out alert of GCLK disconnection	0 (Default)	Enable***
			1	Disable

*Please refer to "Setting the PWM Counting Mode" section.

**Please refer to "TP Function (Thermal Protection)" section.

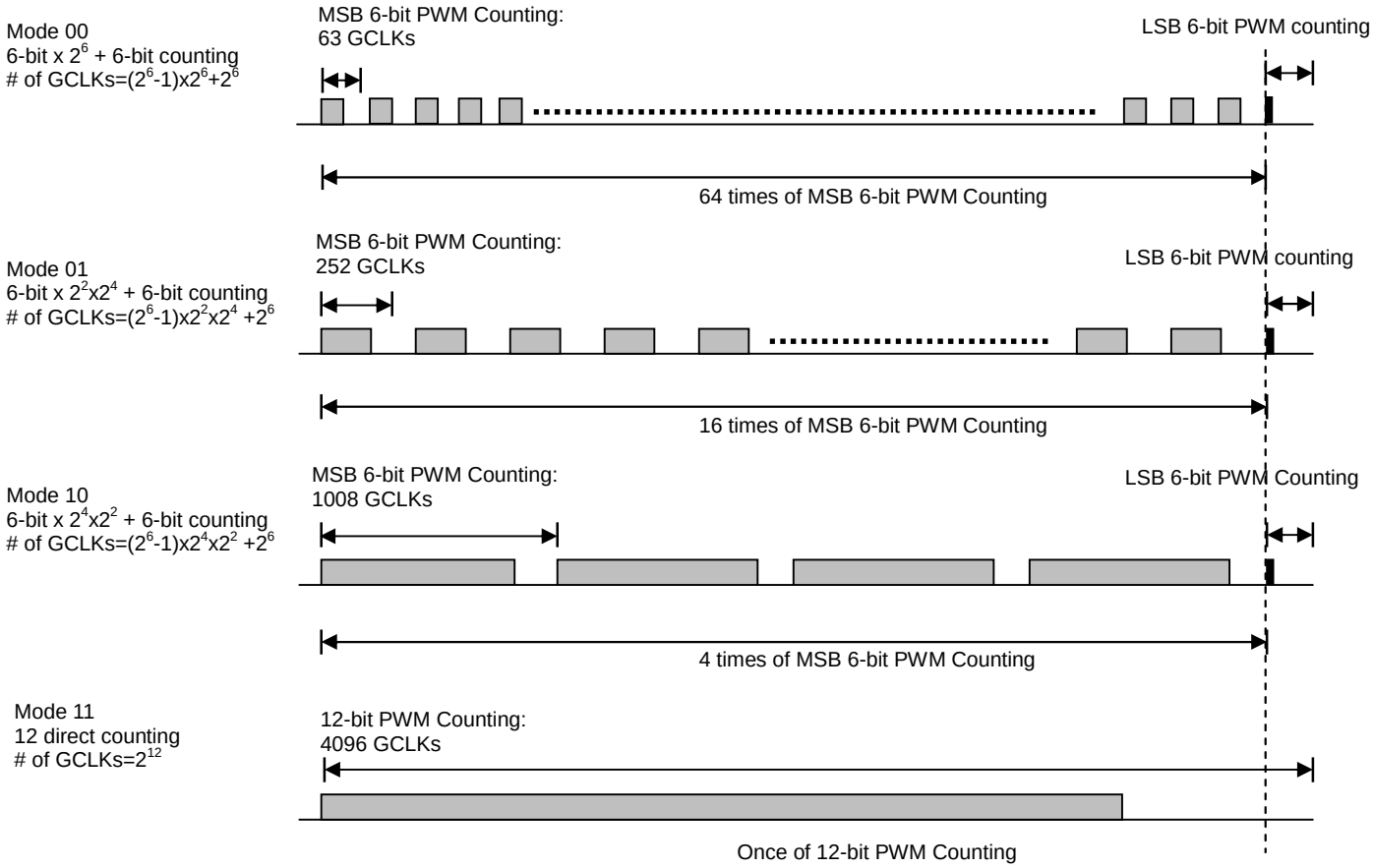
***Please refer to "Time-Out Alert of GCLK Disconnection" section.

Setting the PWM Gray Scale Counter

MBI5031 provides a 12-bit color depth. The value of each 16-bit serial data input will be valid only for 12 bits and implemented according 12-bit PWM counter.

Setting the PWM Counting Mode

MBI5031 defines the different counting algorithms that support S-PWM™, scrambled PWM, technology. With S-PWM™ , the total PWM cycles can be broken down into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution. MBI5031 also allows changing different counting algorithms and provides the better output linearity when there are fewer transitions of output.



: Output ports are “on”.

Synchronization for PWM Counting

Between the data frame and the video frame, when the bit “A” is set to “0”, MBI5031 will automatically handle the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data has finished one internal PWM cycle. It will prevent the lost count of image data resolution and guarantee the data accuracy. In this mode, system controller only needs to provide a continuous running GCLK for PWM counter. The output will be renewed after finishing one of MSB PWM cycles.

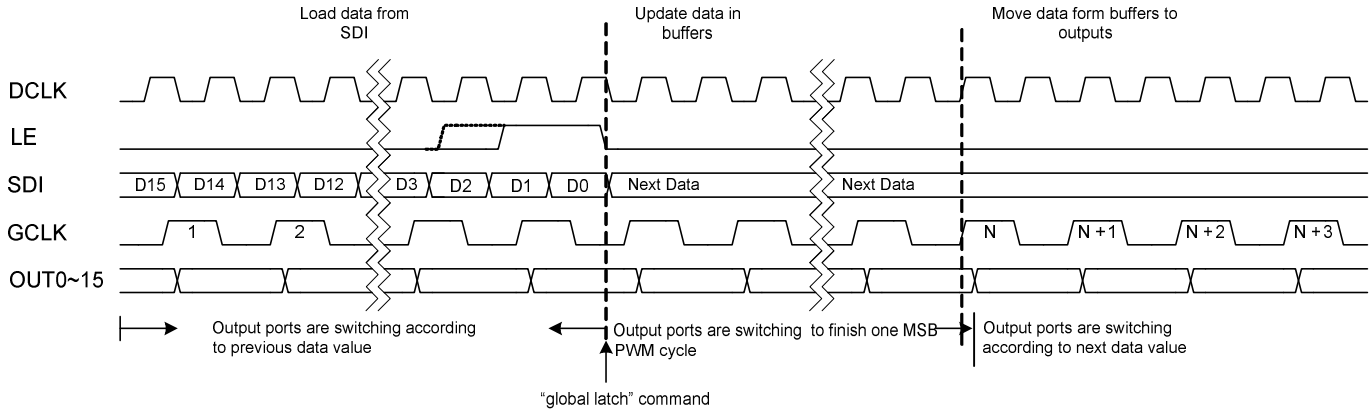


Figure 8

When the bit “A” is set to “1” (Default), MBI5031 will update the next image data into output buffer immediately, no matter the counting status of previous image data is. In this mode, system controller will synchronize the GCLK according image data outside MBI5031 by itself. Otherwise, the conflict of previous image data and next image data will cause the data lost.

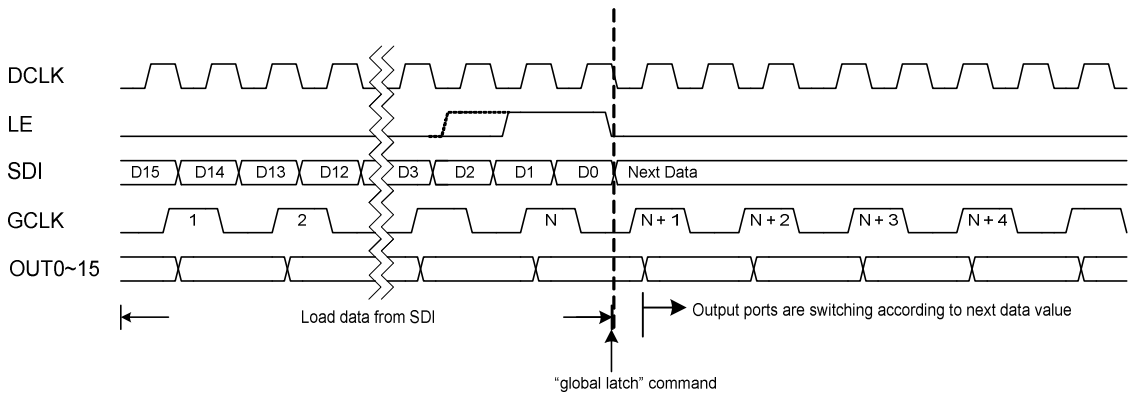


Figure 9

Time-Out Alert of GCLK Disconnection

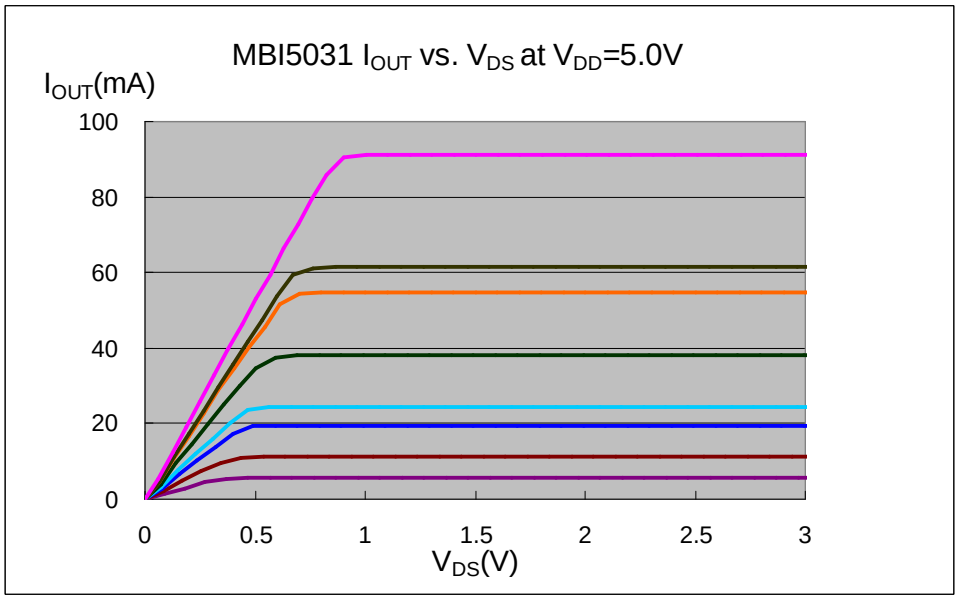
When signal of GCLK is disconnected for around 1 second period, the all output ports will be turned off automatically. This function will protect the LED display system from staying on always and prevent a big current from damaging the power system. The default is set to ‘enable” when bit “0” is 0. When the GCLK is active again and new serial data are moved in, the driver resumes to work after resetting the internal counters and comparators.

Constant Current

In LED display application, MBI5031 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The typical current variation between channels is less than ±1.5%, and that between ICs is less than ±3%.

2) In addition, the current characteristic of output stage is flat and users can refer to the figure as shown below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.



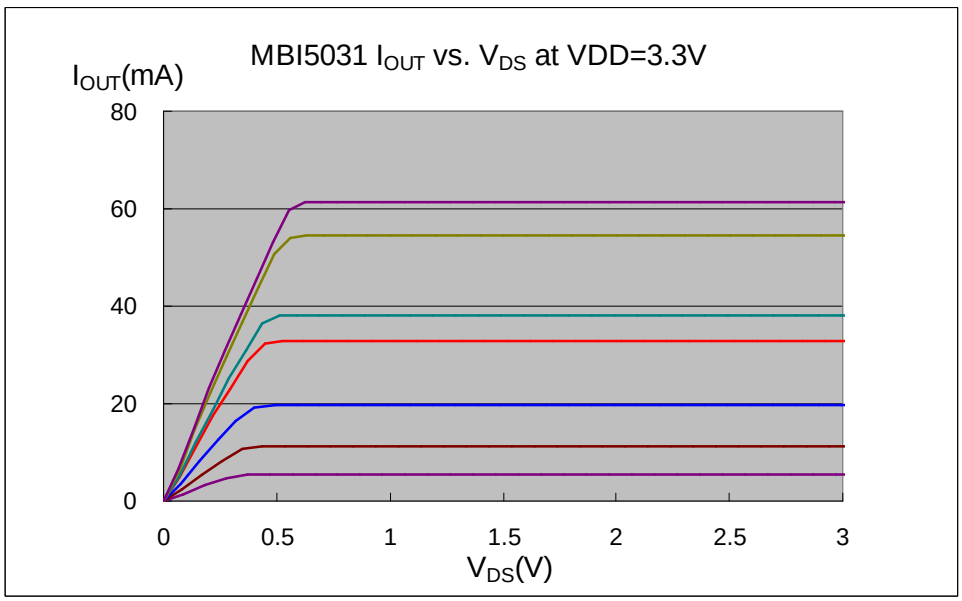


Figure 10

Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

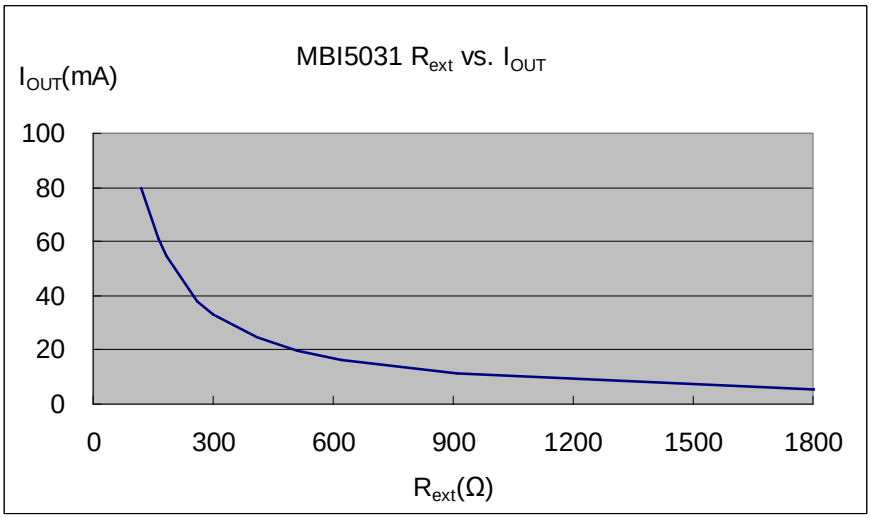


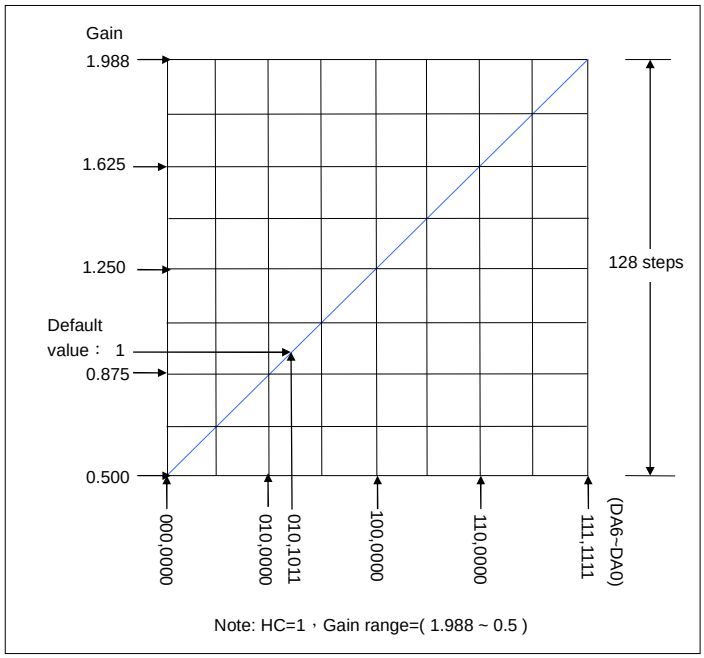
Figure 11

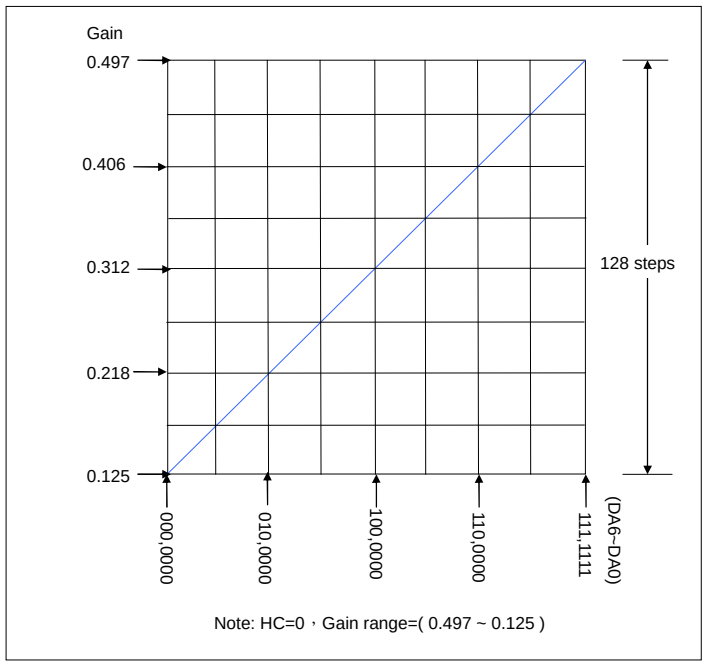
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.63Volt x G; I_{OUT}=($V_{R\text{-}EXT}$/R_{ext})x15.5

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit2 of the configuration register. The default value of G is 1. For your information, the output current is about 21mA when R_{ext}=460Ω and 10.8mA when R_{ext}=910Ω if G is set to default value 1. The formula and setting for G are described in next section.

Current Gain Adjustment





The bit 9 to bit 2 of the configuration register set the gain of output current, i.e., G. As totally 8-bit in number, i.e., ranged from 8'b00000000 to 8'b11111111, these bits allow the user to set the output current gain up to 256 levels. These bits can be further defined inside Configuration Register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA6	DA5	DA4	DA3	DA2	DA1	DA0	-	-

1. Bit 9 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 8 to bit 2 are DA6 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(256G-128)/3

HC=0, D=(1024G-128)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D=DA6x2^6+DA5x2^5+DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 7-bit mantissa DA6~DA0.

For example,

HC=1, G=1.25, D=(256x1.25-128)/3=64

the D in binary form would be:

$D=64=1x2^6+0x2^5+0x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The bit 9 to bit 2 of the configuration register are set to 8'b1100,0000.

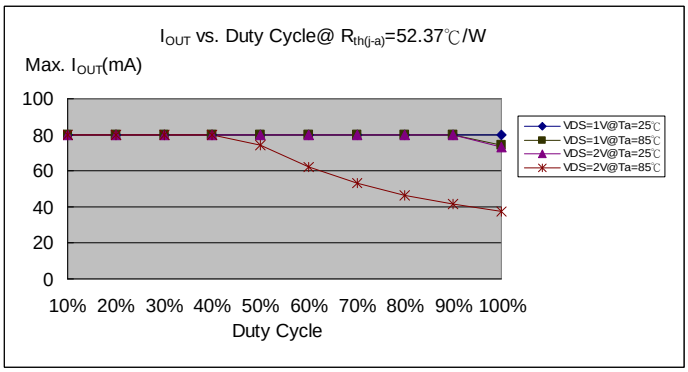
Delay Time of Staggered Output

MBI5031 has a built-in staggered circuit to perform delay mechanism. Among output ports exist a graduated 40ns delay time among $\overline{OUT4n}$, $\overline{OUT4n+1}$, $\overline{OUT4n+2}$, and $\overline{OUT4n+3}$, by which the output ports will be divided to four groups at a different time so that the instant current from the power line will be lowered.

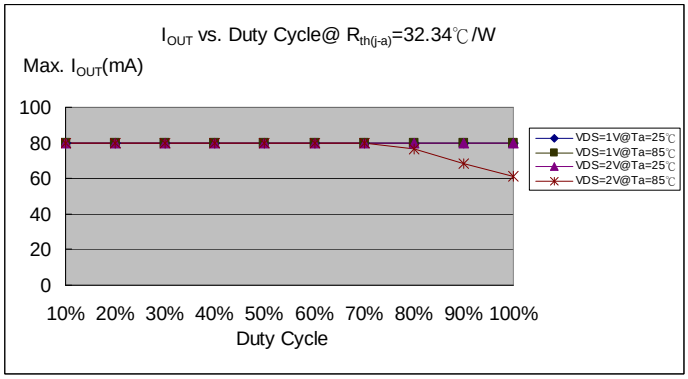
Package Power Dissipation (PD)

The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

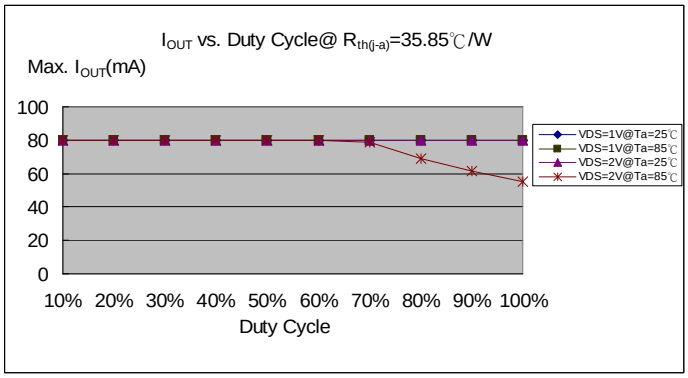
$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.



MBI5031GF



MBI5031GTS



MBI5031GFN

Condition: I_{OUT}=80mA, 16 output channels	
Device Type	$R_{th(j-a)}$ (°C /W)
GF	52.37
GTS	32.34
GFN	35.85

Figure 12

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.

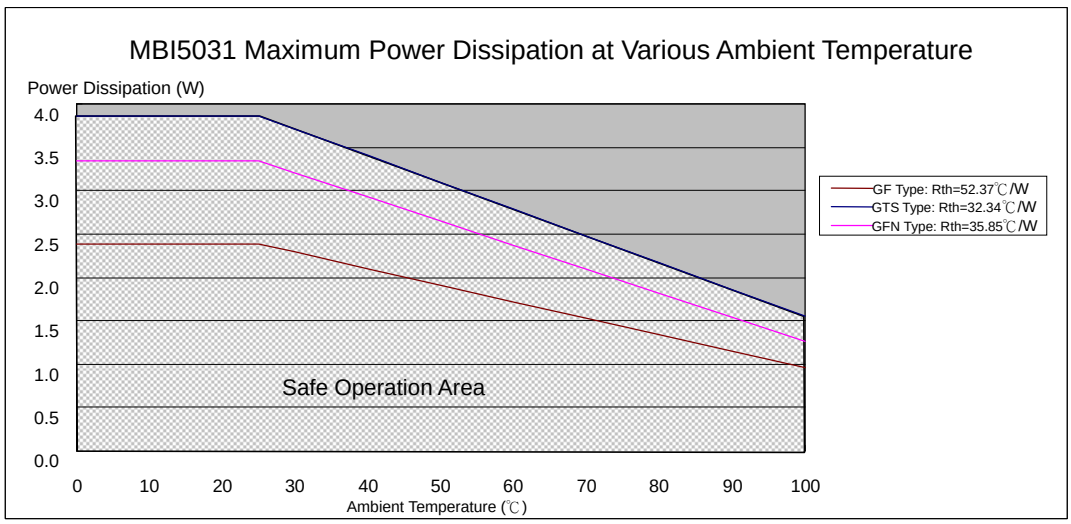


Figure 13

Usage of Thermal Pad

The PCB area L2xW2 is 4 times of the IC's area L1xW1.The thickness of the PCB is 1.6mm, copper foil 1 Oz. The thermal pad on the IC's bottom has to be mounted on the copper foil.

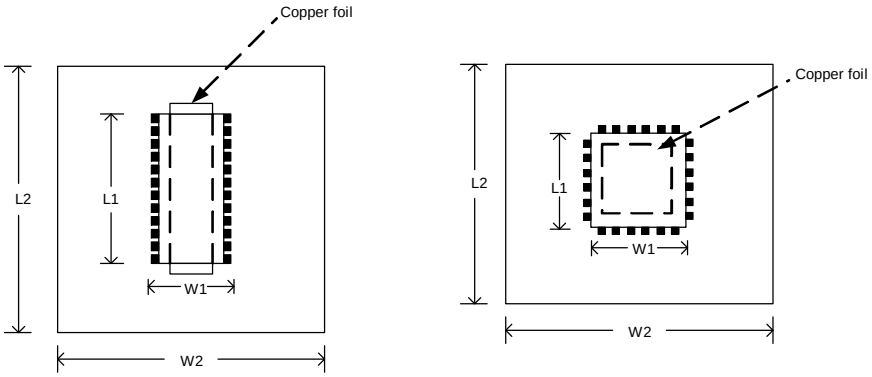


Figure 14

TP Function (Thermal Protection)

The TP function is disable by default when bit "1" is set to "0". If this bit is set to "1" and the junction temperature exceeds the threshold, T_X (150°C typ.), the thermal error flag will be turned on and the TP function will be simultaneously enabled. When the TP function is enabled, the output current will decrease to 25%. As soon as the temperature is below (110°C typ.), the thermal error flag will return to the default value "0" and the output current will recover from the 25% current. The average output current is limited, and therefore, the driver is protected from being overheated, however, it will degrade the gray scale.

LED Supply Voltage (V_{LED})

MBI5031 are designed to operate with V_{DS} ranging from 0.4V to 0.8V (depending on I_{OUT}=5~80mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

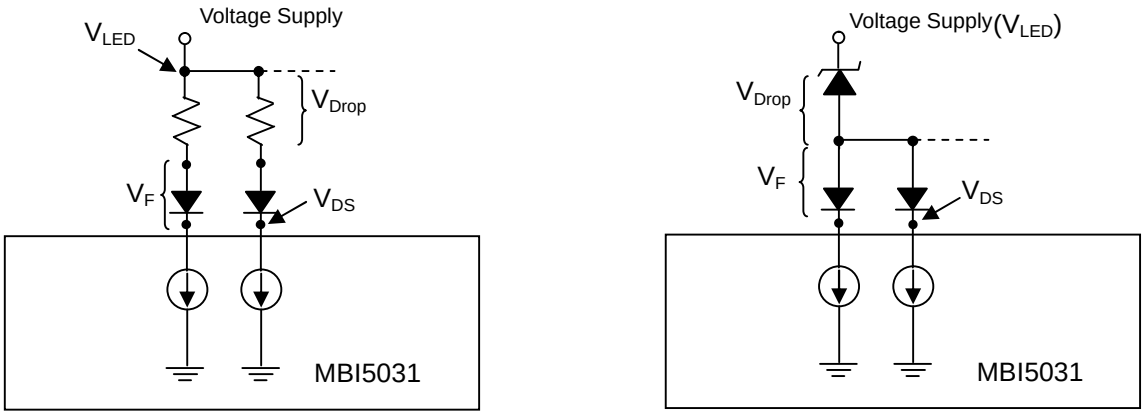
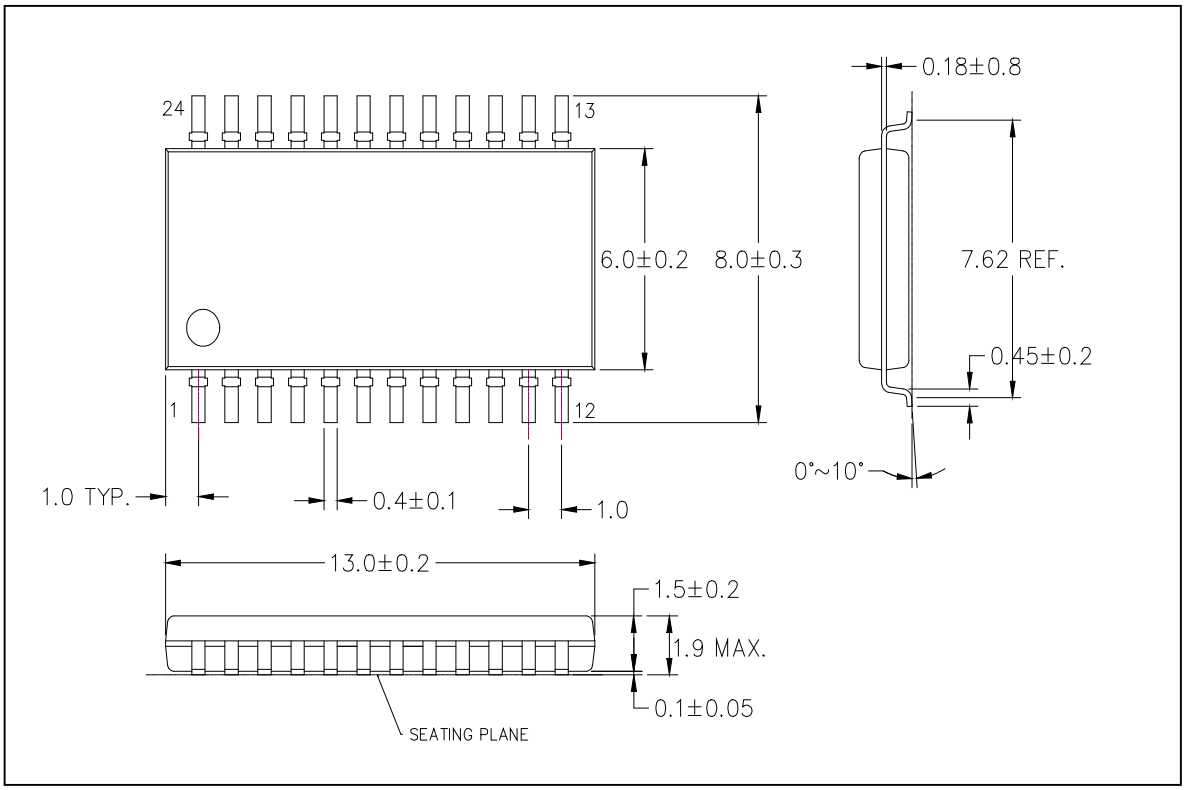


Figure 15

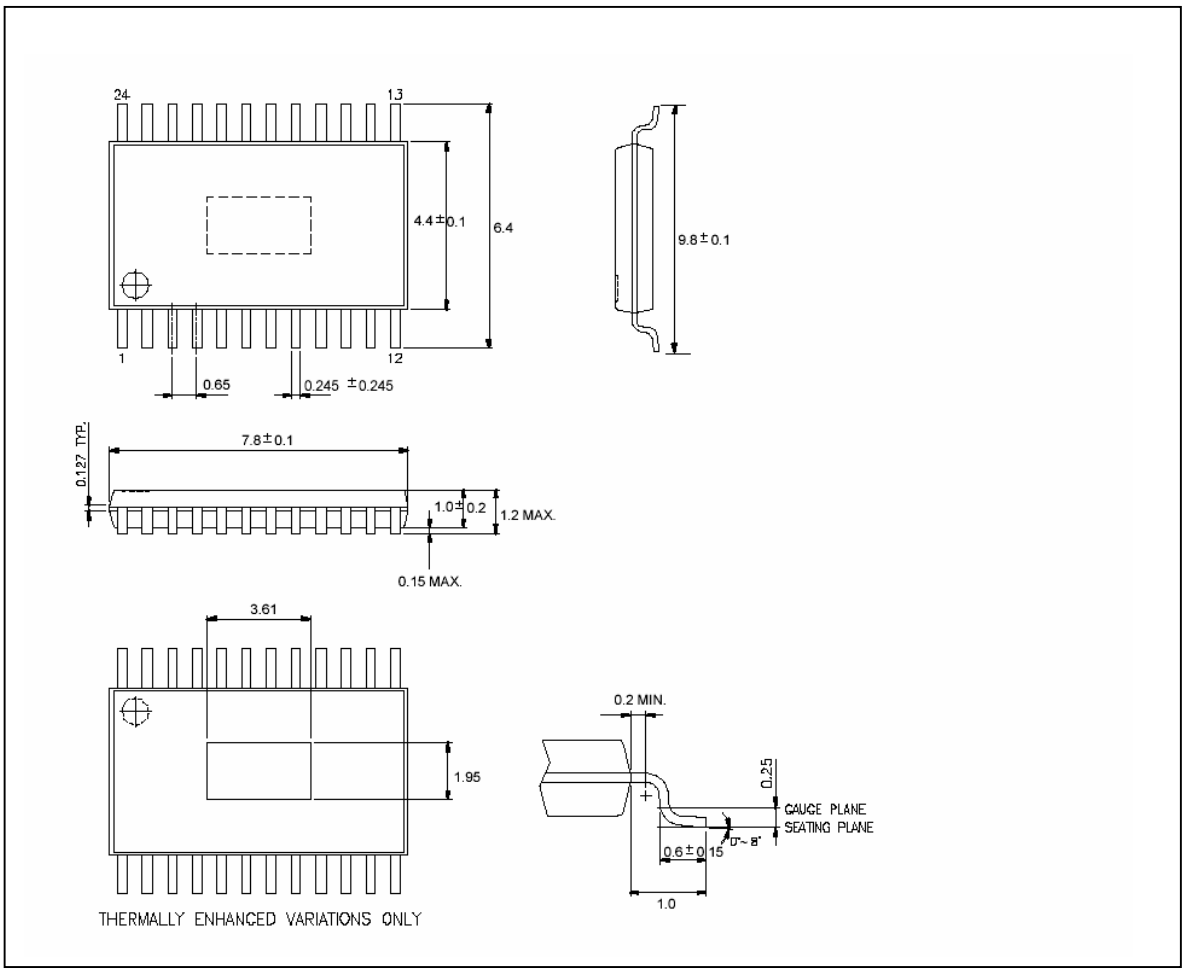
Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers-Overshoot".

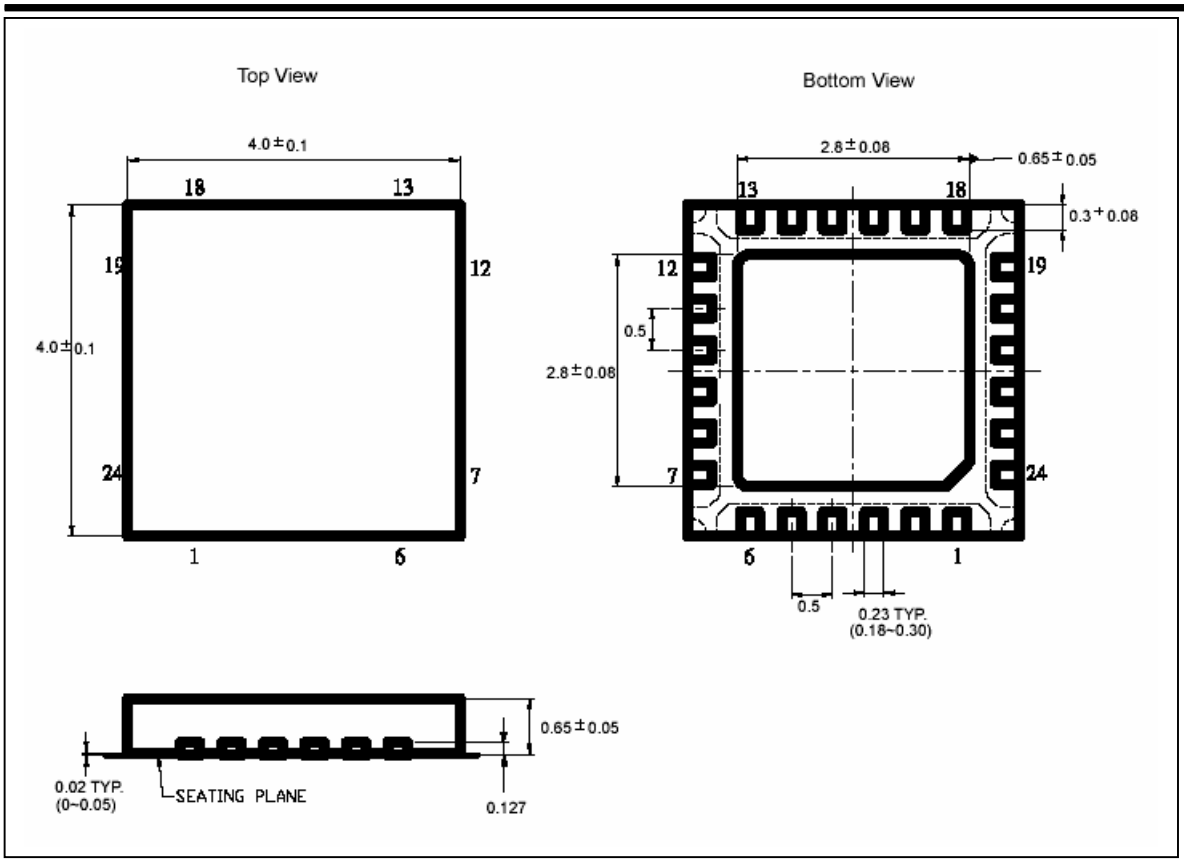
Package Outline



MBI5031GF Outline Drawing



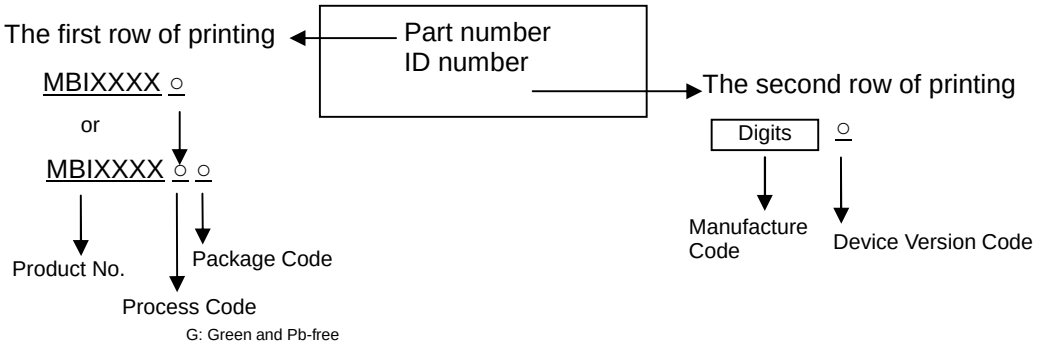
MBI5031GTS Outline Drawing



MBI5031GFN Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top Mark Information



Product Revision History

Datasheet version	Device Version Code
V1.00	A
V2.00	B

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5031GF	SOP24-300-1.00	0.30
MBI5031GTS	TSSOP24-173 -0.65	0.0967
MBI5031GFN	QFN24-4*4- 0.5	0.0379

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